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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M97A

MLB

SCHEMATIC

REFERENCED FROM T18

03/11/2009

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6

5

4

3

2

1

REV

ZONE

ECN

DESCRIPTION OF CHANGE

CK APPD

ENG APPD

C

681298

PRODUCTION RELEASED

03/11/09

?

POST-RAMP

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7918	1	SCHEM, MLB, M97A	SCH	CRITICAL	
820-2327	1	PCBF, MLB, M97	PCB	CRITICAL	

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DIMENSIONS ARE IN MILLIMETERS

XX ±

X.XX ±

X.XXX ±

ANGLES ±

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER

ENG APPD

QA APPD

RELEASE

MATERIAL/FINISH NOTED AS APPLICABLE

DESIGN CK

MFG APPD

DESIGNER

SCALE

SIZE

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TITLE

SCHEM, MLB, M97A

DRAWING NUMBER

051-7918

REV.

C

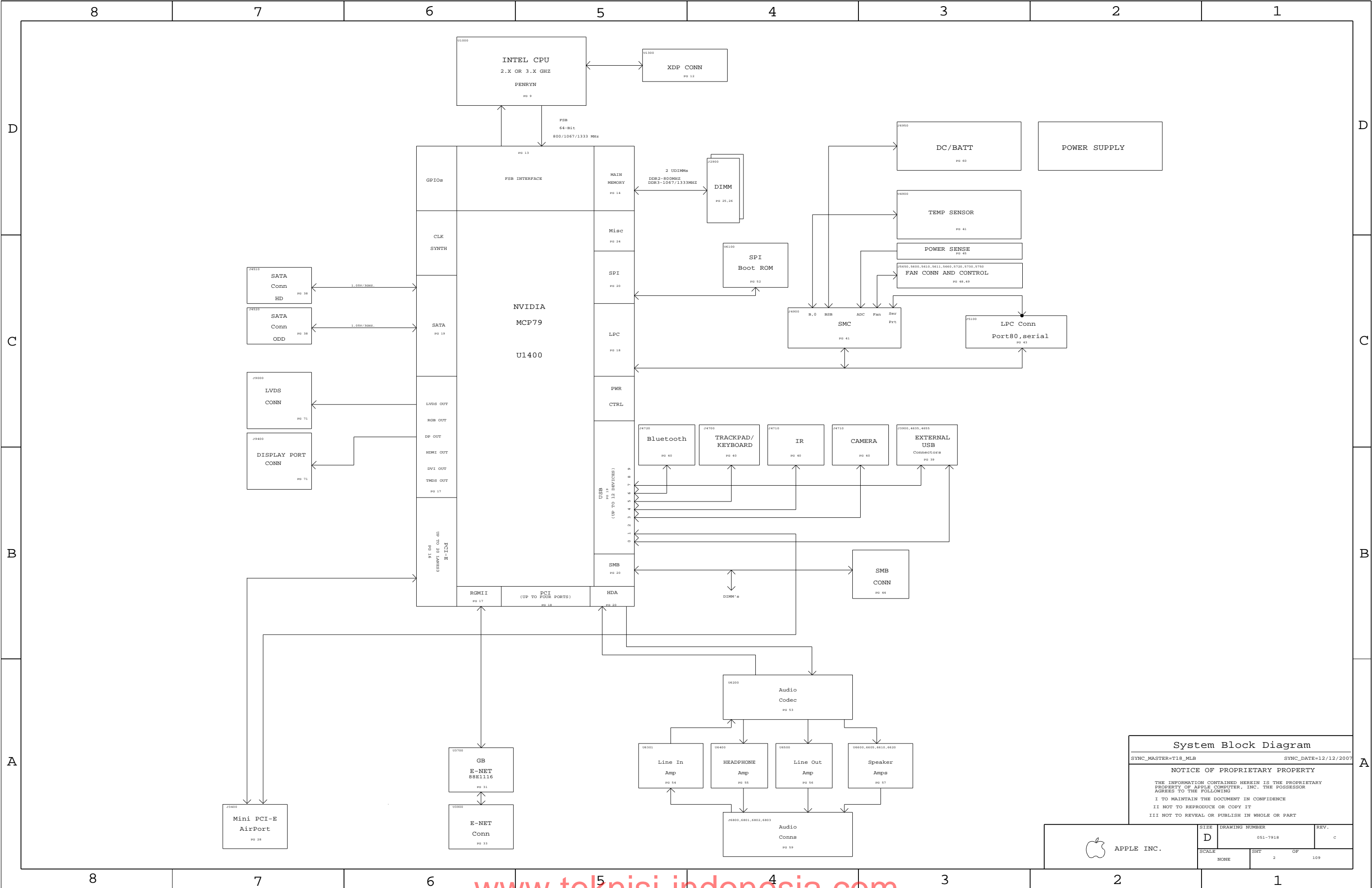
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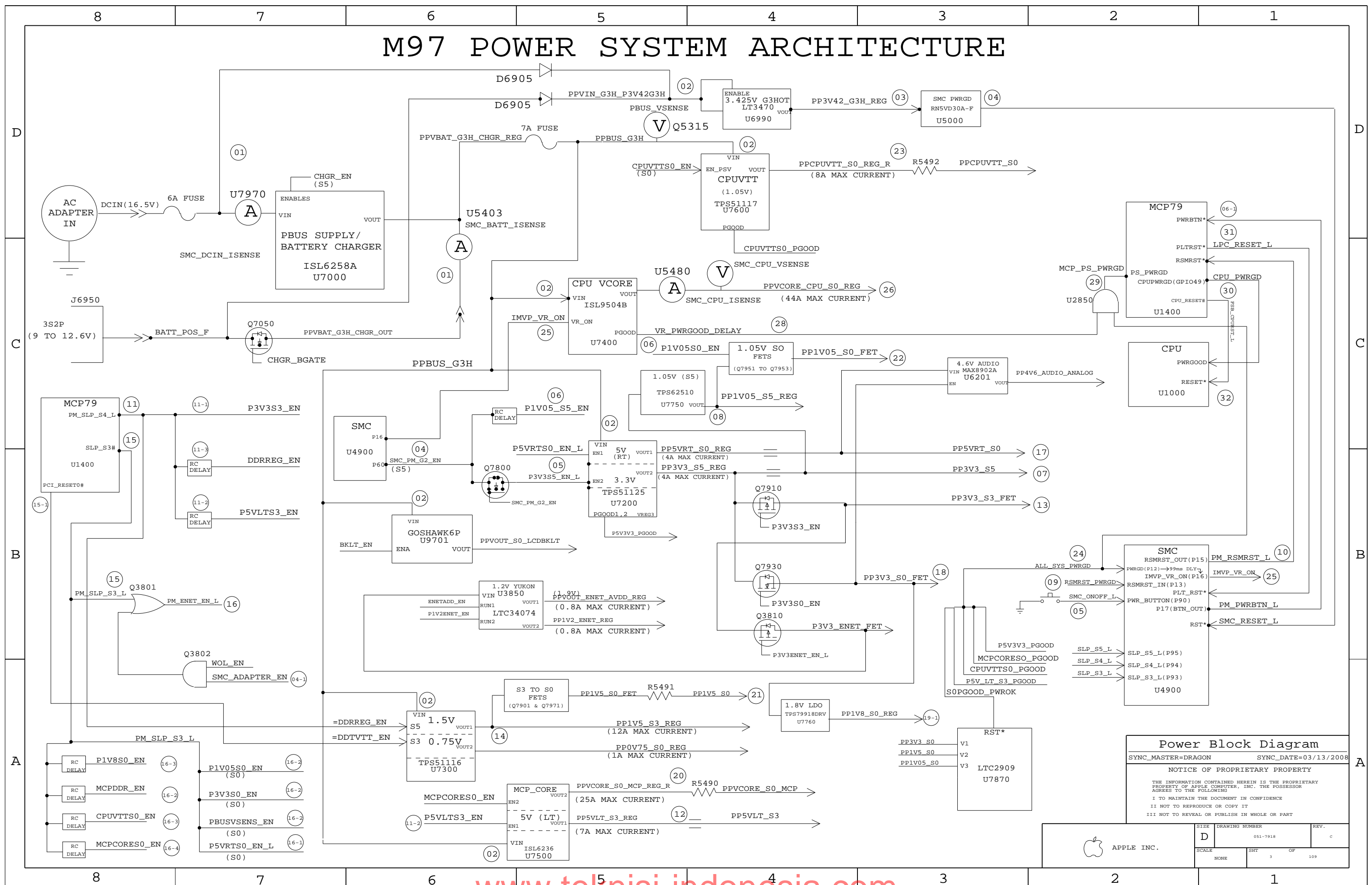
www.teknisi-indonesia.com



System Block Diagram		
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SYNC_DATE=12/12/2007		
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## M97 POWER SYSTEM ARCHITECTURE





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Revision History															
BOM CHANGES FROM M97:															
<div><div></div><div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></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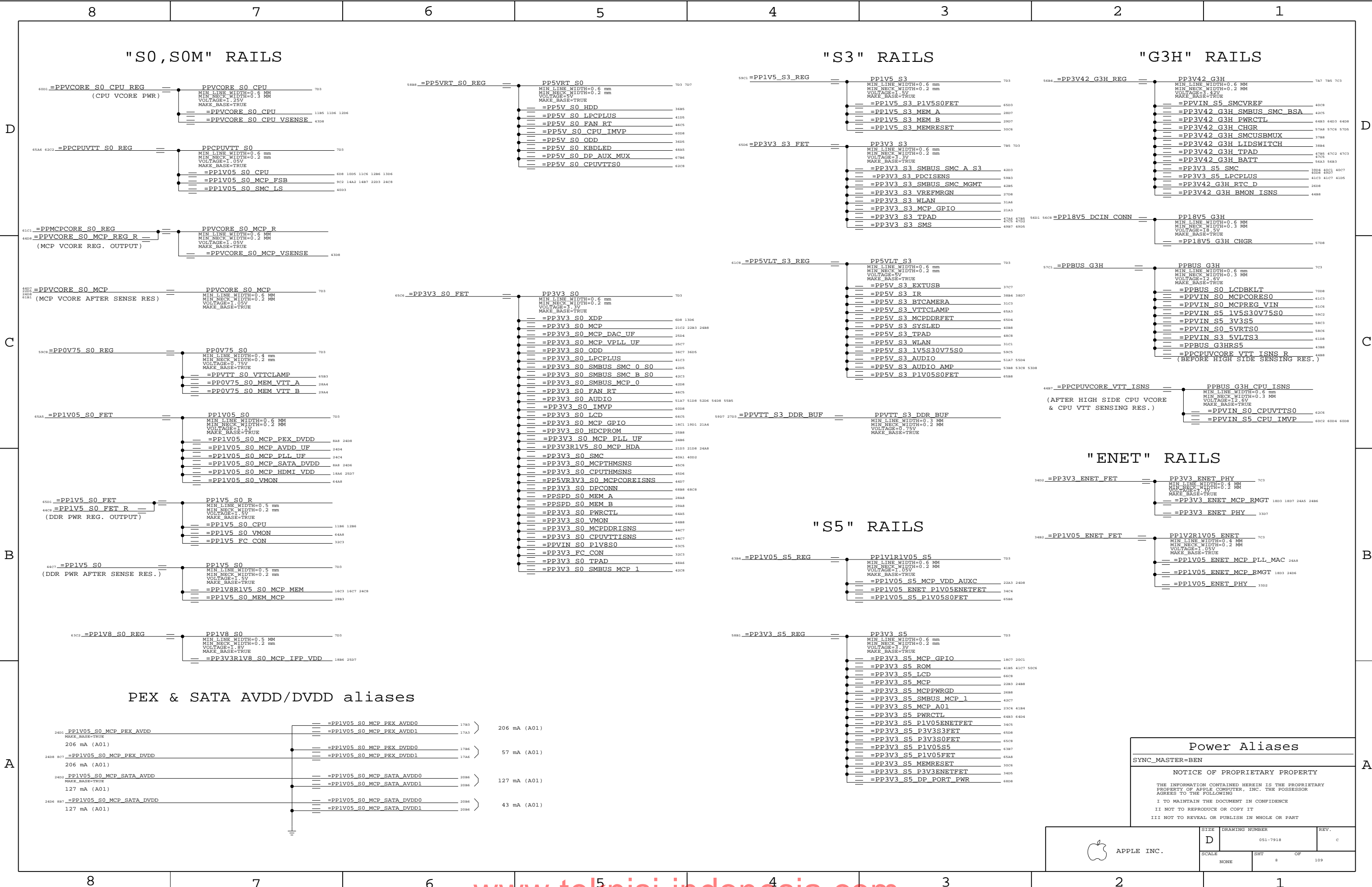
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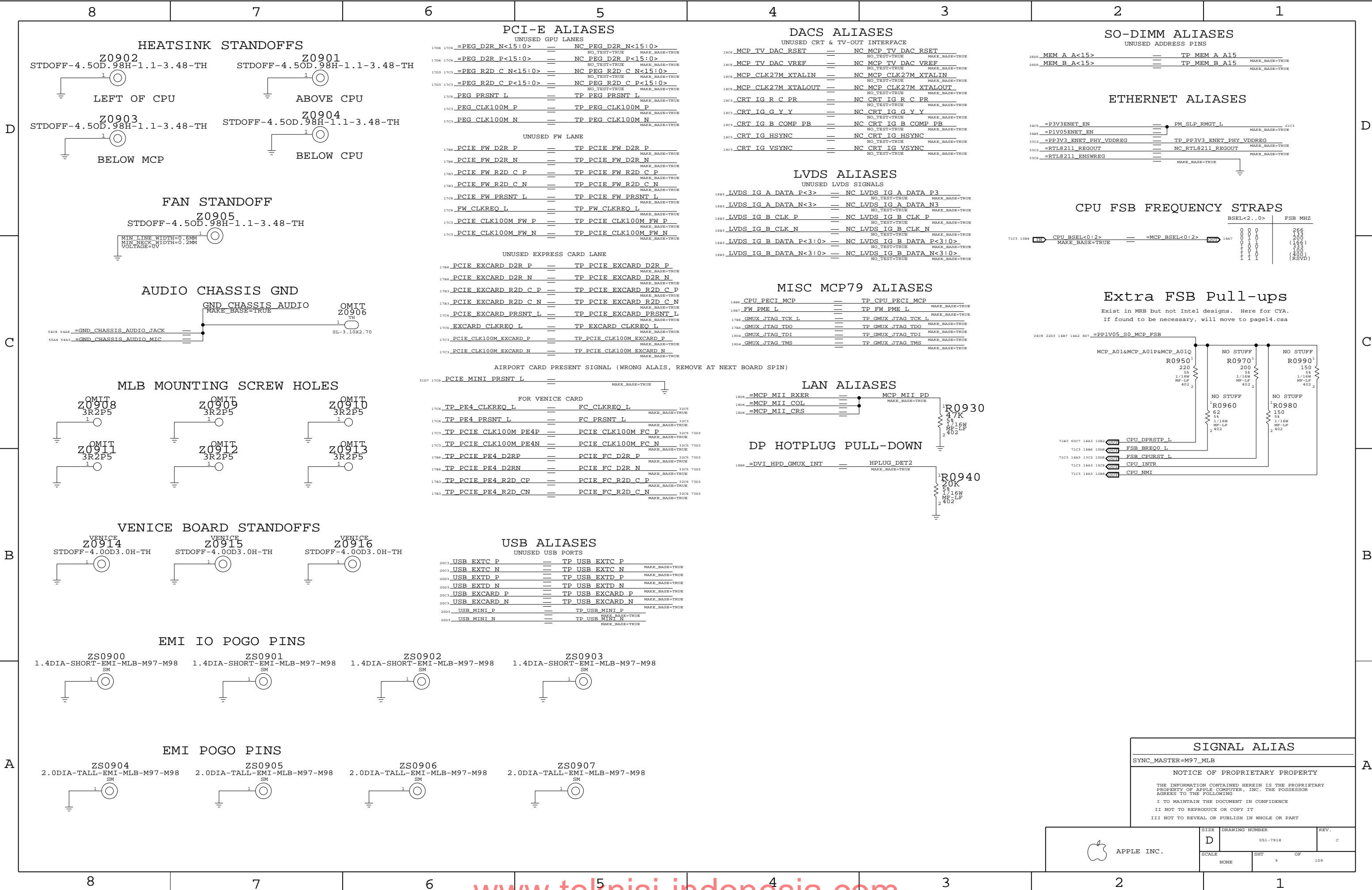
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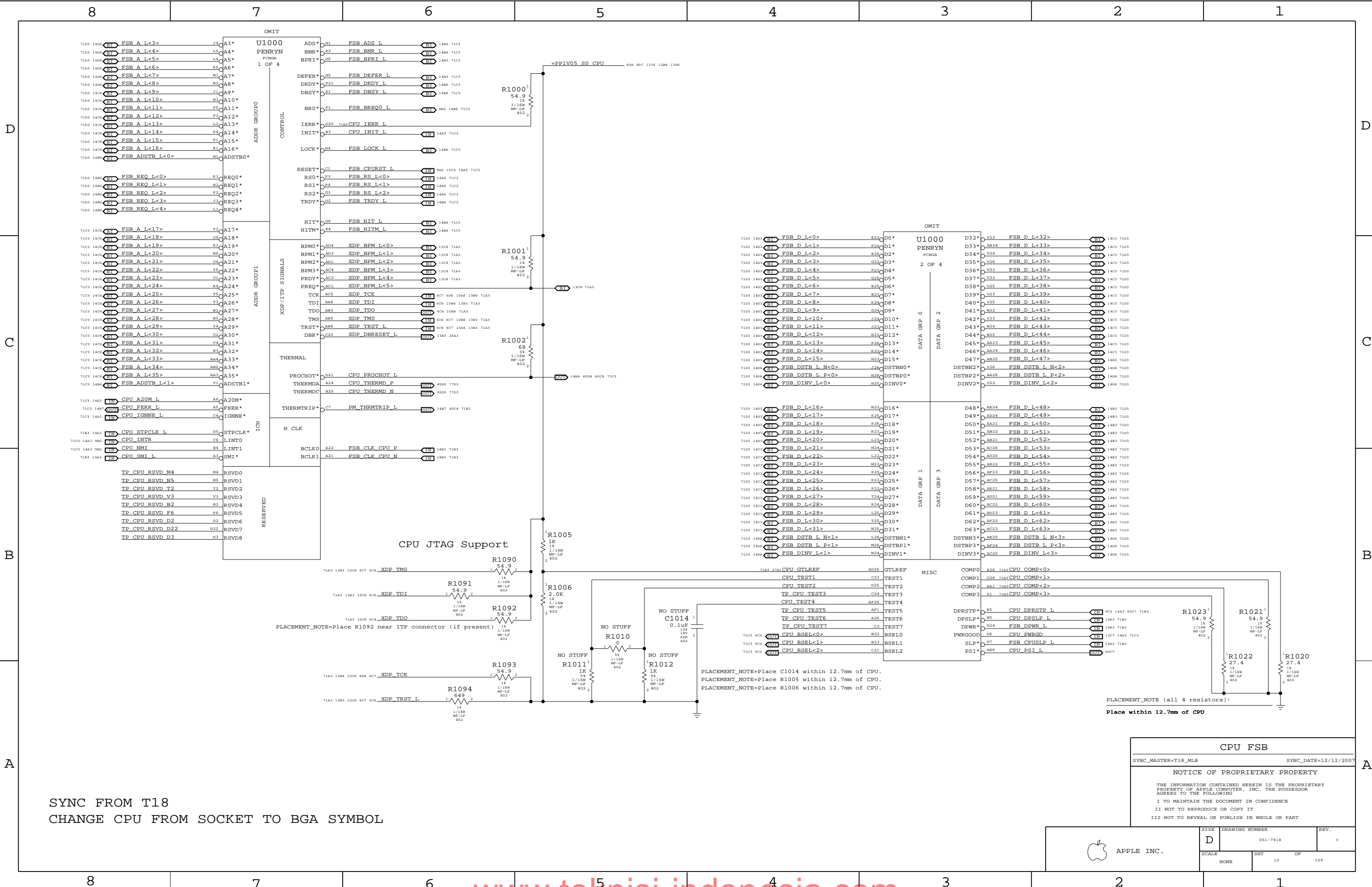
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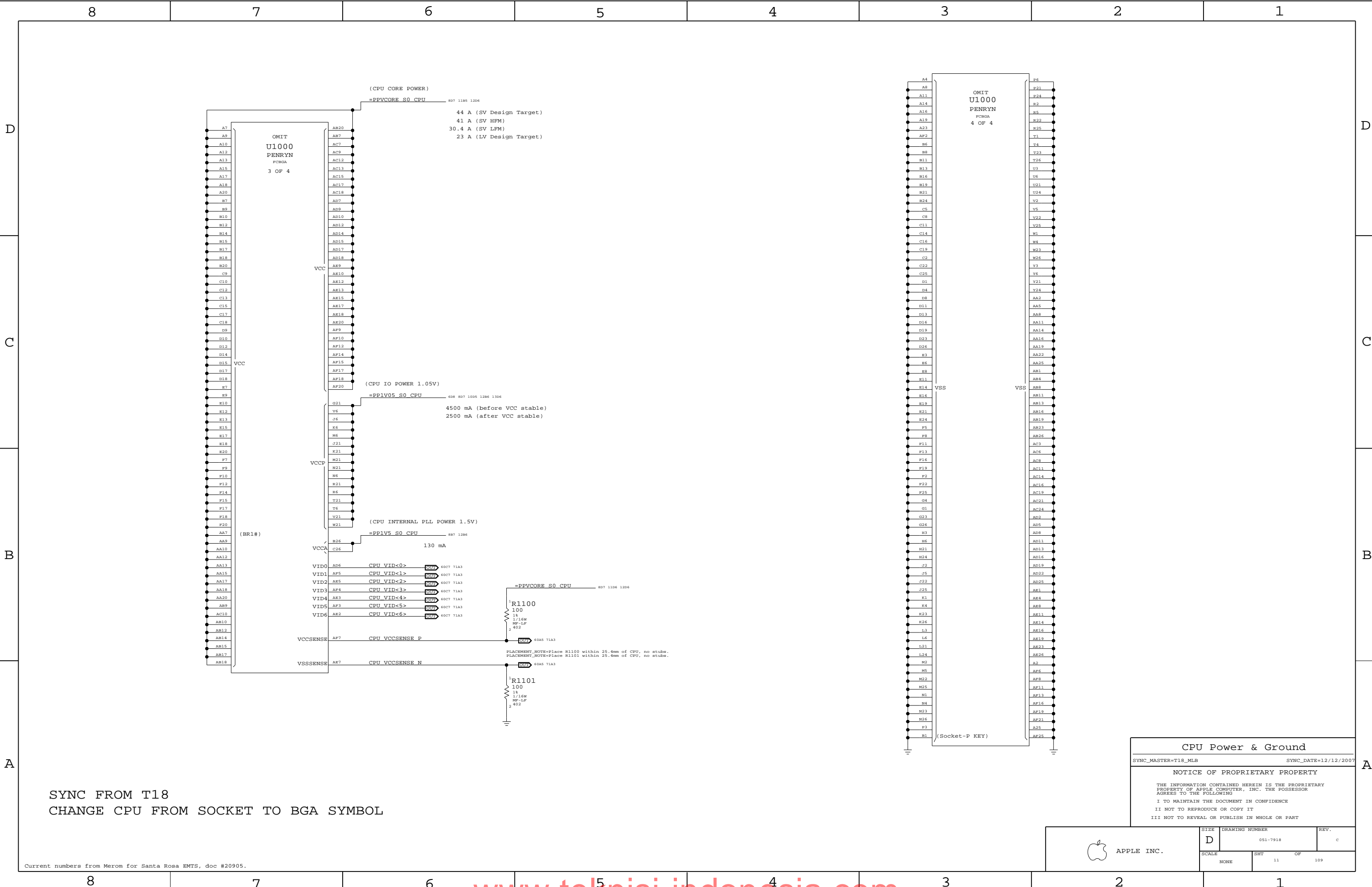
8		7		6		5		4		3		2		1						
Functional Test Points																				
D	Fan Connectors				RIGHT CLUTCH CONN				DEBUG VOLTAGE											
	1889	TRUE	PP5VRT_S0	(NEED 3 TP) 703 805	1889	TRUE	PP5V_S3_BT CAMERA_F	3107	1889	TRUE	PPVCORE_S0_CPU	807				D				
	1885	TRUE	FAN_RT_PWM	4684	1889	TRUE	PCIE_MINI_D2R_P	1786 3107 7303	1889	TRUE	PPCPUVTT_S0	807								
	1815	TRUE	FAN_RT_TACH	46C4	1889	TRUE	PCIE_MINI_D2R_N	1786 3107 7303	1889	TRUE	PPVCORE_S0_MCP	807								
	(NEED TO ADD 3 GND TP)				1889	TRUE	PCIE_MINI_R2D_P	3107 7303	1889	TRUE	PP0V75_S0	807								
	MIC_FUNC_TEST				1889	TRUE	PCIE_MINI_R2D_N	3107 7303	1889	TRUE	PP1V05_S0	807								
	1837	TRUE	MIC_HI_CONN	5481 54D2	1889	TRUE	PCIE_CLK100M_MINI_CONN_P	3107 7303	1889	TRUE	PP1V5_S0	887								
	1835	TRUE	MIC_LO_CONN	5481 54D2	1889	TRUE	PCIE_CLK100M_MINI_CONN_N	3107 7303	1889	TRUE	PP1V8_S0	887								
	1835	TRUE	MIC_SHLD_CONN	54D2 55A6	1889	TRUE	USB_CAMERA_CONN_P	3187 74C3	1889	TRUE	PP5VRT_S0	7D7 8D5								
	SPEAKER_FUNC_TEST				1889	TRUE	USB_CAMERA_CONN_N	3187 74C3	1889	TRUE	PP3V3_S0	8C5								
1899	TRUE	SPKRAMP_L_N_OUT	5382 54D2	1889	TRUE	PP5V_WLAN	703 31C5	1889	TRUE	PP1V5_S3	8D3									
C	1899	TRUE	SPKRAMP_L_P_OUT	5382 54D2	1889	TRUE	PCIE_WAKE_L	1786 23C5 31C7	1889	TRUE	PP3V3_S3	785 8D3								
	1829	TRUE	SPKRAMP_R_N_OUT	53C3 54C2	1889	TRUE	SMBUS_SMC_A_S3_SCL	785 42D2 76D3	1889	TRUE	PP5VLT_S3	8C3								
	1829	TRUE	SPKRAMP_R_P_OUT	53C3 54C2	1889	TRUE	SMBUS_SMC_A_S3_SDA	785 42D2 76D3	1889	TRUE	PP1V1R1V05_S5	8B3								
	1899	TRUE	SPKRAMP_SUB_N_OUT	5382 54C2	1889	TRUE	CONN_USB2_BT_P	3187 74C3	1889	TRUE	PP3V3_S5	8B3								
	1899	TRUE	SPKRAMP_SUB_P_OUT	53C2 54C2	1889	TRUE	CONN_USB2_BT_N	3187 7483	1889	TRUE	PP3V42_G3H	7A7 785 8D1								
	1829	TRUE	SPKRAMP_SUB_P_OUT	53C2 54C2	1889	TRUE	MINI_CLKREQ_O_L	31C7	1889	TRUE	PPBUS_G3H	8C1								
	THERMAL_FUNC_TEST				1889	TRUE	MINI_RESET_CONN_L	31A7	1889	TRUE	PP3V3_ENET_PHY	8B1								
	1899	TRUE	MCPHTMSNS_D2_P	4585 77D3	1889	TRUE	(NEED TO ADD 3 GND TP)		1889	TRUE	PP1V2R1V05_ENET	8B1								
	1899	TRUE	MCPHTMSNS_D2_N	4585 77D3	1889	TRUE	SATA_HDD_CONN	(NEED 4 TP)	1889	TRUE	PP3V3_G3_RTC	21C8 22A5 26D4								
	LVDS_FUNC_TEST				1889	TRUE	PP5V_S0_HDD_FLT	7C3 36B7	1889	TRUE	PP5V_WLAN	7D5 31C5								
B	1825	TRUE	PP3V3_LCDVDD_SW_F	7C3 66C2	1889	TRUE	SATA_HDD_R2D_P	36A7 73A3	1889	TRUE	PP5V_SW_ODD	787 36D3								
	1835	TRUE	PP3V3_S0_LCD_F	66C3	1889	TRUE	SATA_HDD_R2D_N	36A7 73A3	1889	TRUE	PP5V_S0_HDD_FLT	7C5 36B7								
	1825	TRUE	PPVOUT_S0_LCDBKLT	7C3 66B2 69B3 69C1	1889	TRUE	SATA_HDD_D2R_C_P	36A7 73A3	1889	TRUE	PP3V3_S5_AVREF_SMC	39D4 40C6								
	1825	TRUE	LVDS_IG_DDC_CLK	18B3 66C5	1889	TRUE	SATA_HDD_D2R_C_N	36A7 73A3	1889	TRUE	PP18V5_S3	7C5 48C1 48D3								
	1825	TRUE	LVDS_IG_DDC_DATA	18B3 66C5	1889	TRUE	SATA_ODD_R2D_N	787 36C5 73A3	1889	TRUE	PP3V3_S3_LDO	7C5 48B4 48C3								
	1825	TRUE	LVDS_IG_A_DATA_N<0>	18B3 66C2 73B3	1889	TRUE	(NEED TO ADD 4 GND TP)		1889	TRUE	PP3V3_LCDVDD_SW_F	7C7 66C2								
	1825	TRUE	LVDS_IG_A_DATA_P<0>	18B3 66C2 73B3	1889	TRUE	IPD_FLEX_CONN		1889	TRUE	PPVOUT_S0_LCDBKLT	7C7 66B2 69B3 69C1								
	1825	TRUE	LVDS_IG_A_DATA_P<1>	18B3 66C2 73B3	1889	TRUE	PP3V3_S3_LDO	7C3 48B4 48C3	1889	TRUE	BKL_VREF_4V9	49B6 49B8 49C4 49C8								
	1825	TRUE	LVDS_IG_A_DATA_P<2>	18B3 66C2 73B3	1889	TRUE	PP18V5_S3	7C3 48C1 48D3	1889	TRUE	PP4V6_AUDIO_ANALOG	51A3 51D3 52D6								
	1825	TRUE	LVDS_IG_A_DATA_N<1>	18B3 66C2 73B3	1889	TRUE	TPAD_GND_F	48B4 48C3 48C4 48C7	1889	TRUE	SMC_PM_G2_EN	39D5 64D8								
A	1825	TRUE	LVDS_IG_A_DATA_P<2>	18B3 66C2 73B3	1889	TRUE	Z2_CS_L	47C8 48C3	1889	TRUE	PM_SLP_S4_L	21C3 39C5 40A2 64C8								
	1825	TRUE	LVDS_IG_A_DATA_N<2>	18B3 66C2 73B3	1889	TRUE	Z2_DEBUG3	47C8 48C3	1889	TRUE	PM_SLP_S3_L	21C3 34B7 39C5 41A5 64D5 68D8								
	1825	TRUE	LVDS_IG_A_DATA_P<2>	18B3 66C2 73B3	1889	TRUE	Z2_MOSI	47C8 48C3	1889	(NEED TO ADD 4 GND TP)										
	1825	TRUE	LVDS_IG_A_CLK_F_N	66C2 73B3	1889	TRUE	Z2_MISO	47C8 48C3	1889											
	1825	TRUE	LVDS_IG_A_CLK_F_P	66C2 73B3	1889	TRUE	Z2_SCLK	47C8 48C3	1889											
	1825	TRUE	LED_RETURN_1	66B3 69C1	1889	TRUE	Z2_BOOST_EN	48C3 48C5	1889											
	1825	TRUE	LED_RETURN_2	66B3 69C1	1889	TRUE	Z2_HOST_INTN	47D8 48C3	1889											
	1825	TRUE	LED_RETURN_3	66B3 69B1	1889	TRUE	Z2_BOOT_CFG1	47C8 48C3	1889											
	1825	TRUE	LED_RETURN_4	66B3 69B1	1889	TRUE	Z2_CLKIN	47C6 48C3	1889											
	1825	TRUE	LED_RETURN_5	66B3 69B1	1889	TRUE	Z2_KEY_ACT_L	47C8 48C1	1889											
1825	TRUE	LED_RETURN_6	66B3 69B1	1889	TRUE	Z2_RESET	47C8 48C1	1889												
FUNCH TEST																				
SYNC_MASTER=M97_MLB																				
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APPLE INC.										SIZE	DRAWING NUMBER	REV.								
										D	051-7918	C								
										SCALE	SHT	OF								
										NONE	7	109								







SYNC FROM T18  
CHANGE CPU FROM SOCKET TO BGA SYMBOL



SYNC FROM T18  
CHANGE CPU FROM SOCKET TO BGA SYMBOL

CPU Power & Ground

SYNC\_MASTER=T18\_MLB

SYNC\_DATE=12/12/2007

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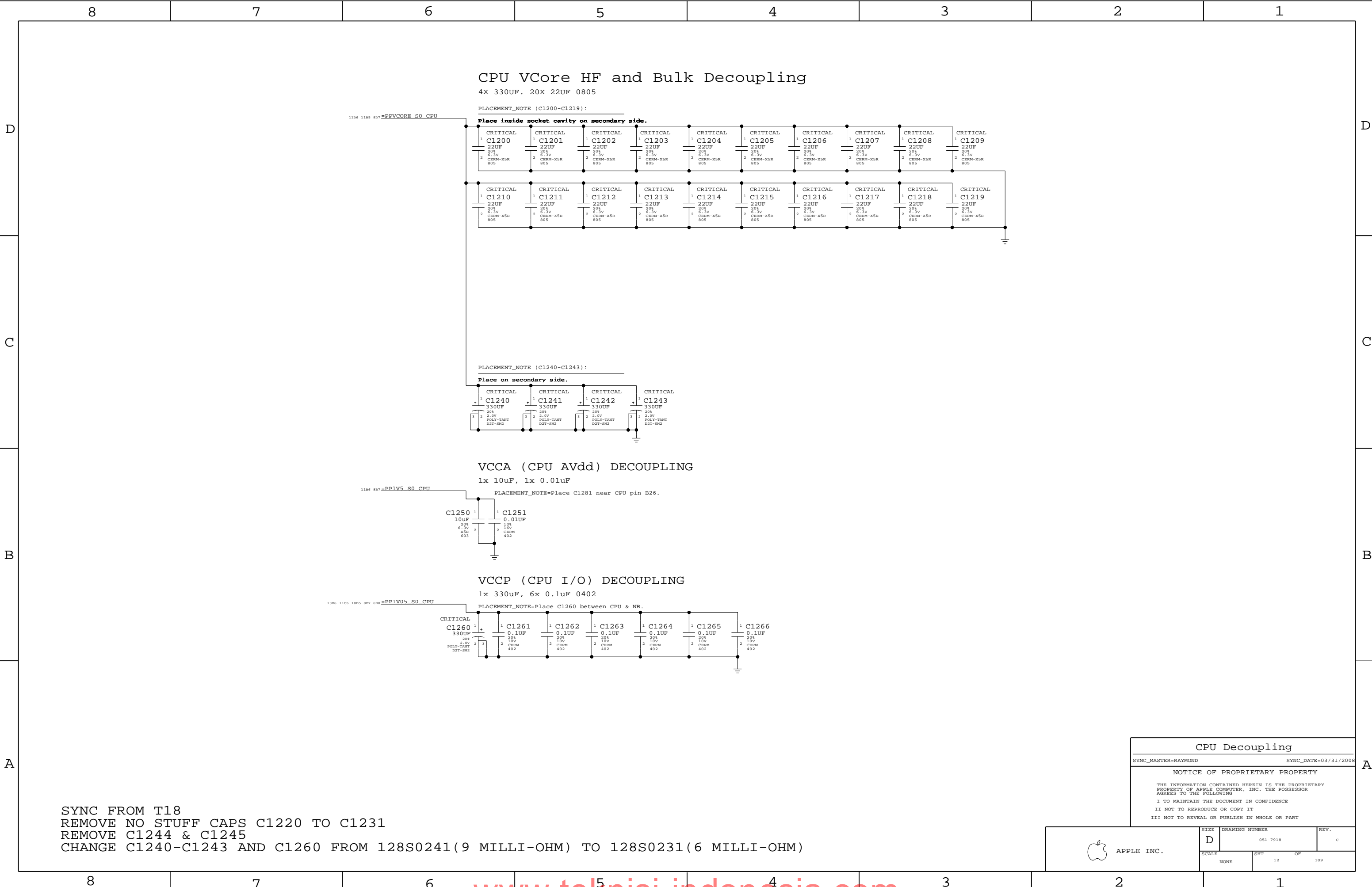
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	D	051-7918		c
SCALE		SHT	OF	REV.
NONE		11	109	



SYNC FROM T18  
REMOVE NO STUFF CAPS C1220 TO C1231  
REMOVE C1244 & C1245  
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

CPU Decoupling

SYNC\_MASTER=RAYMOND

SYNC\_DATE=03/31/2008

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APPLE INC.	SIZE D	DRAWING NUMBER 051-7918	REV. C
	SCALE NONE	SHT 12	OF 109

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B

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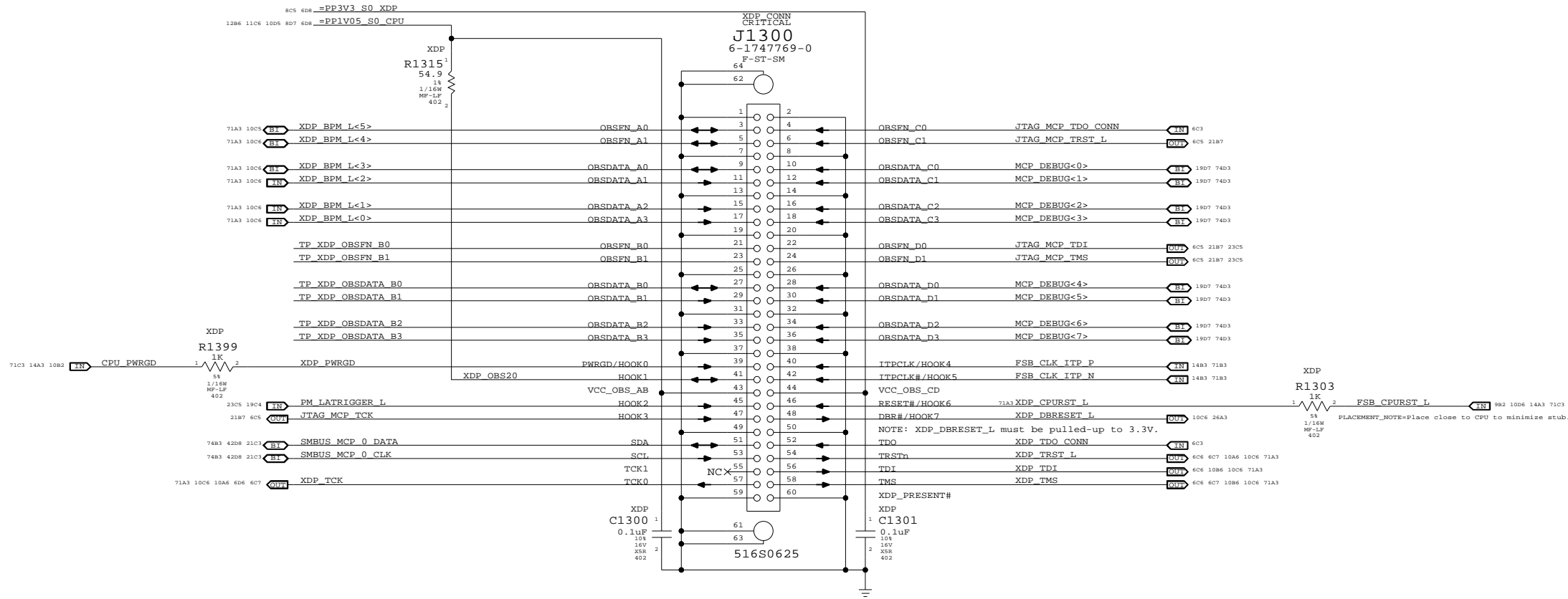
D

C

B

A

MCP79-specific pinout



SYNC FROM T18  
CHANGE STANDARD XDP CONNECTOR TO SMALLER ONE 516S0625  
RENAME JTAG\_MCP\_TDO TO JTAG\_MCP\_TDO\_CONN  
RENAME XDP\_TDO TO XDP\_TDO\_CONN

eXtended Debug Port (XDP)

SYNC\_MASTER=T18\_MLBSYNC\_DATE=12/12/2007

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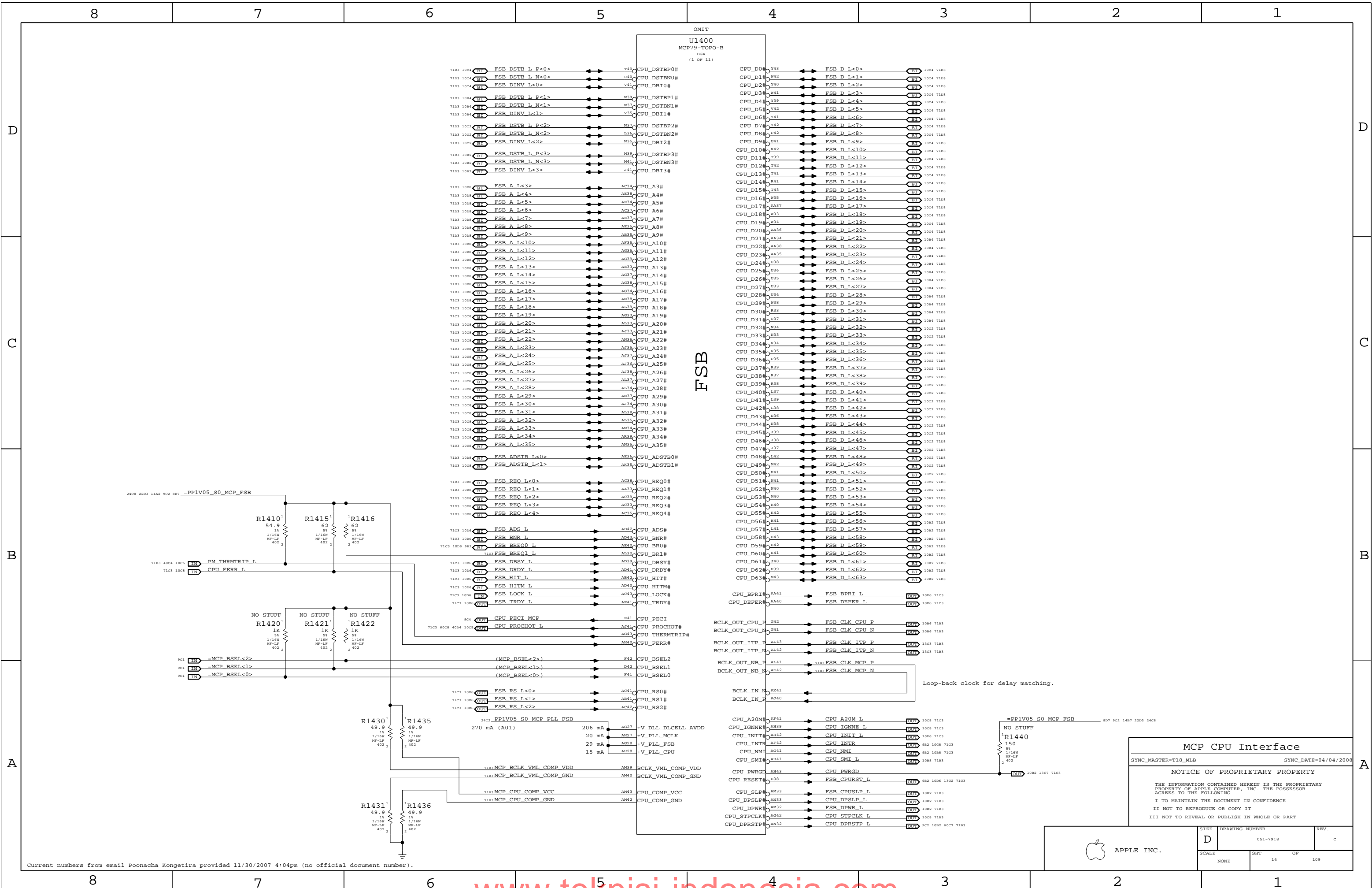
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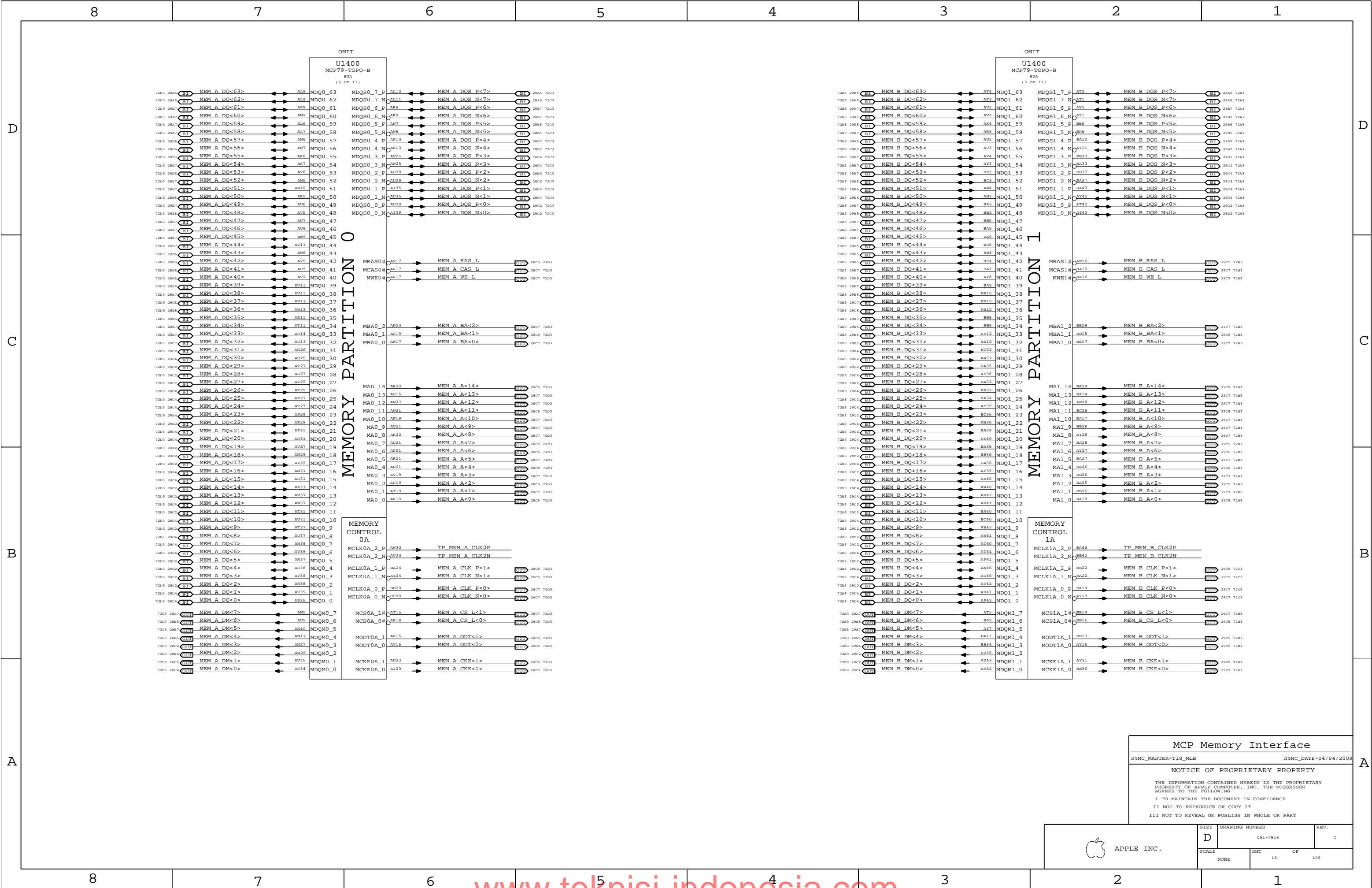
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NONE		13	109





MCP Memory Interface

SYNC\_MASTER=T18\_MLB

SYNC\_DATE=04/04/2008

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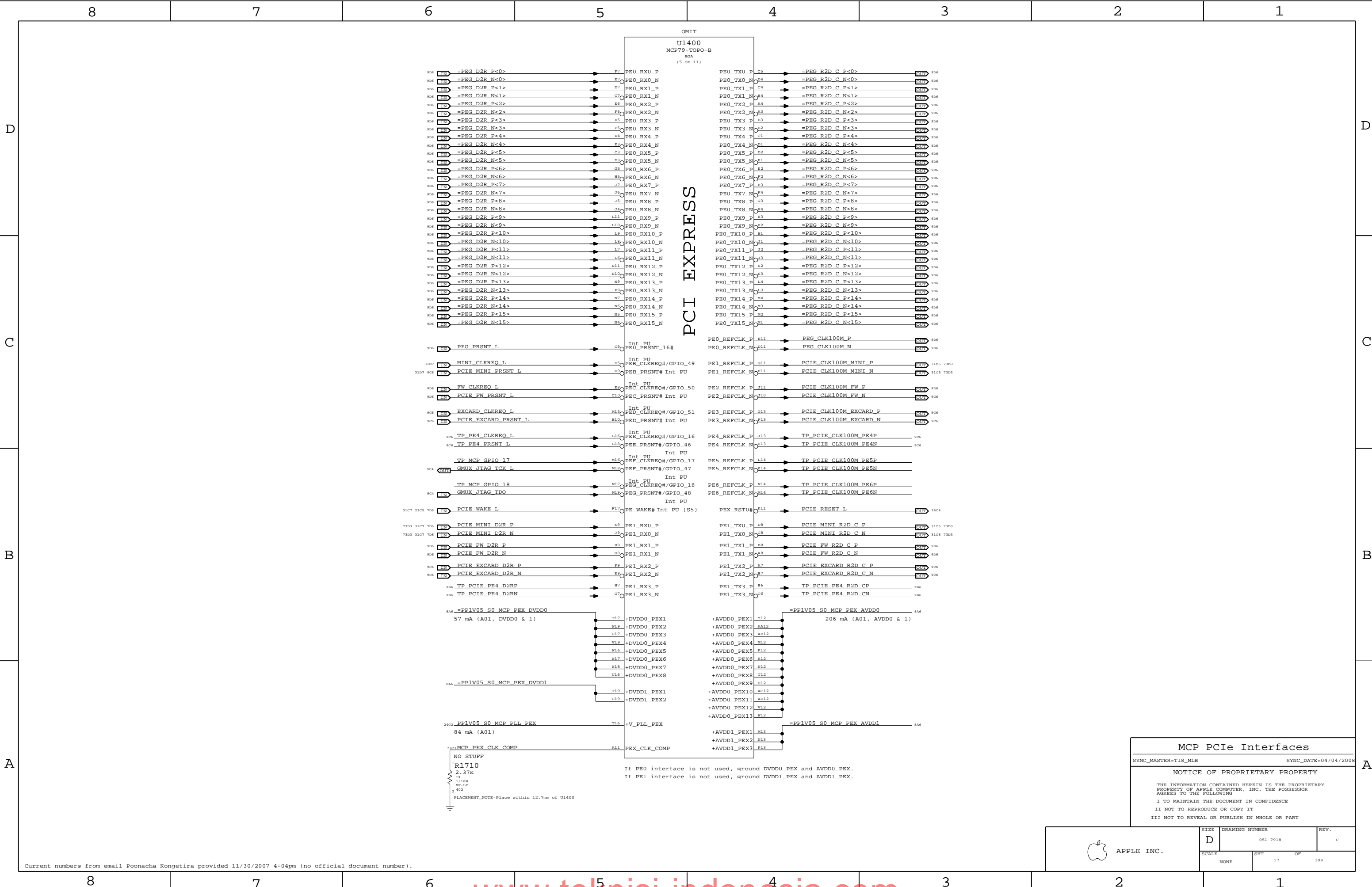
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		15	109





MCP PCIe Interfaces

SYNC\_MASTER=T18\_MLB

SYNC\_DATE=04/04/2008

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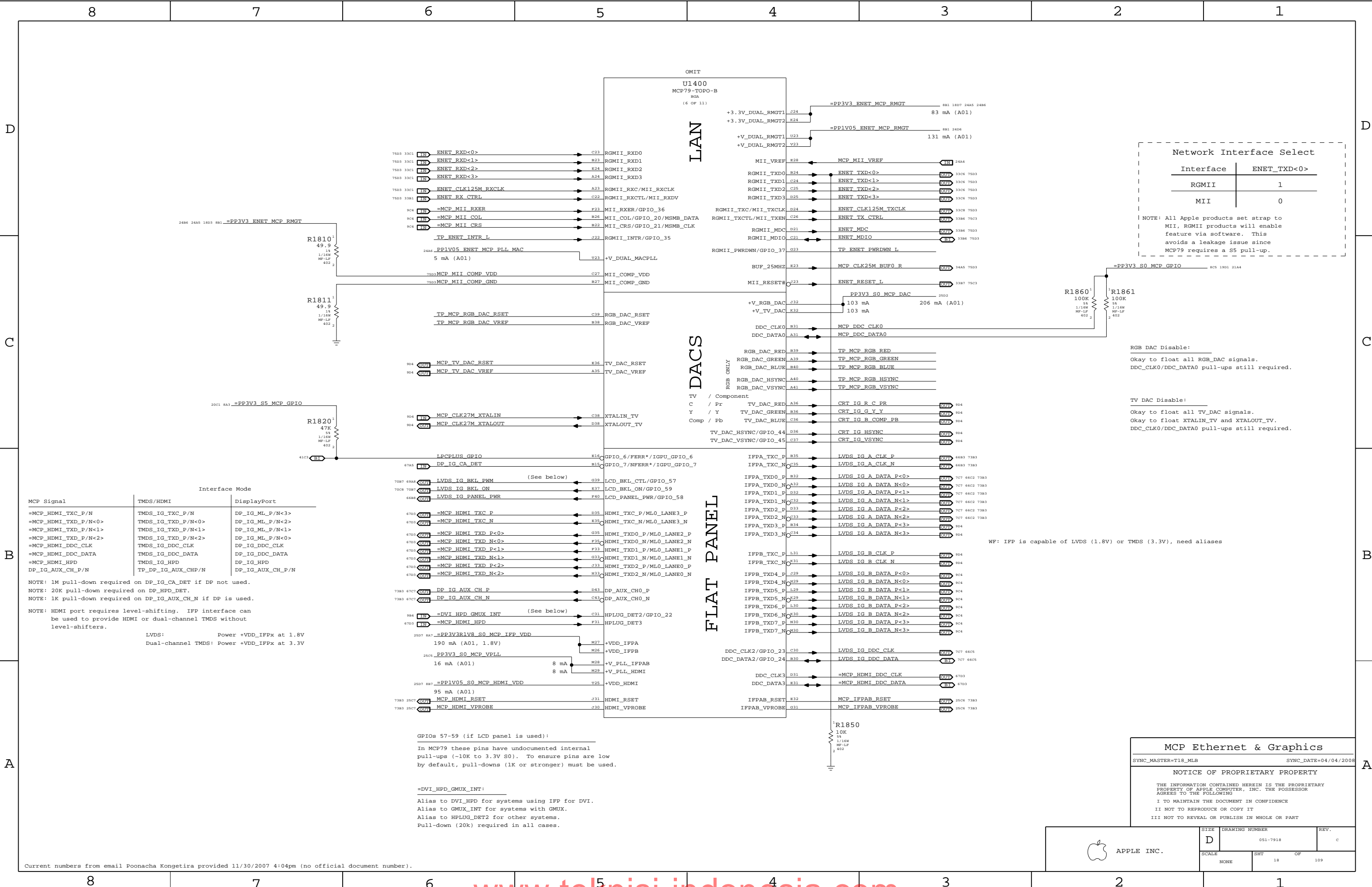
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SCALE		SHT	OF
NONE		17	109



Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable: \_\_\_\_\_  
Okay to float all RGB\_DAC signals.  
DDC\_CLK0/DDC\_DATA0 pull-ups still required.

TV DAC Disable: \_\_\_\_\_  
Okay to float all TV\_DAC signals.  
Okay to float XTALIN\_TV and XTALOUT\_TV.  
DDC\_CLK0/DDC\_DATA0 pull-ups still required.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP\_IG\_CA\_DET if DP not used.  
NOTE: 20K pull-down required on DP\_HPD\_DET.  
NOTE: 1K pull-down required on DP\_IG\_AUX\_CH\_N if DP is used.  
NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD\_IFPx at 1.8V  
Dual-channel TMDS: Power +VDD\_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):  
In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI\_HPD\_GMUX\_INT:  
Alias to DVI\_HPD for systems using IFP for DVI.  
Alias to GMUX\_INT for systems with GMUX.  
Alias to HPLUG\_DET2 for other systems.  
Pull-down (20k) required in all cases.

MCP Ethernet & Graphics

SYNC\_MASTER=T18\_MLB SYNC\_DATE=04/04/2008

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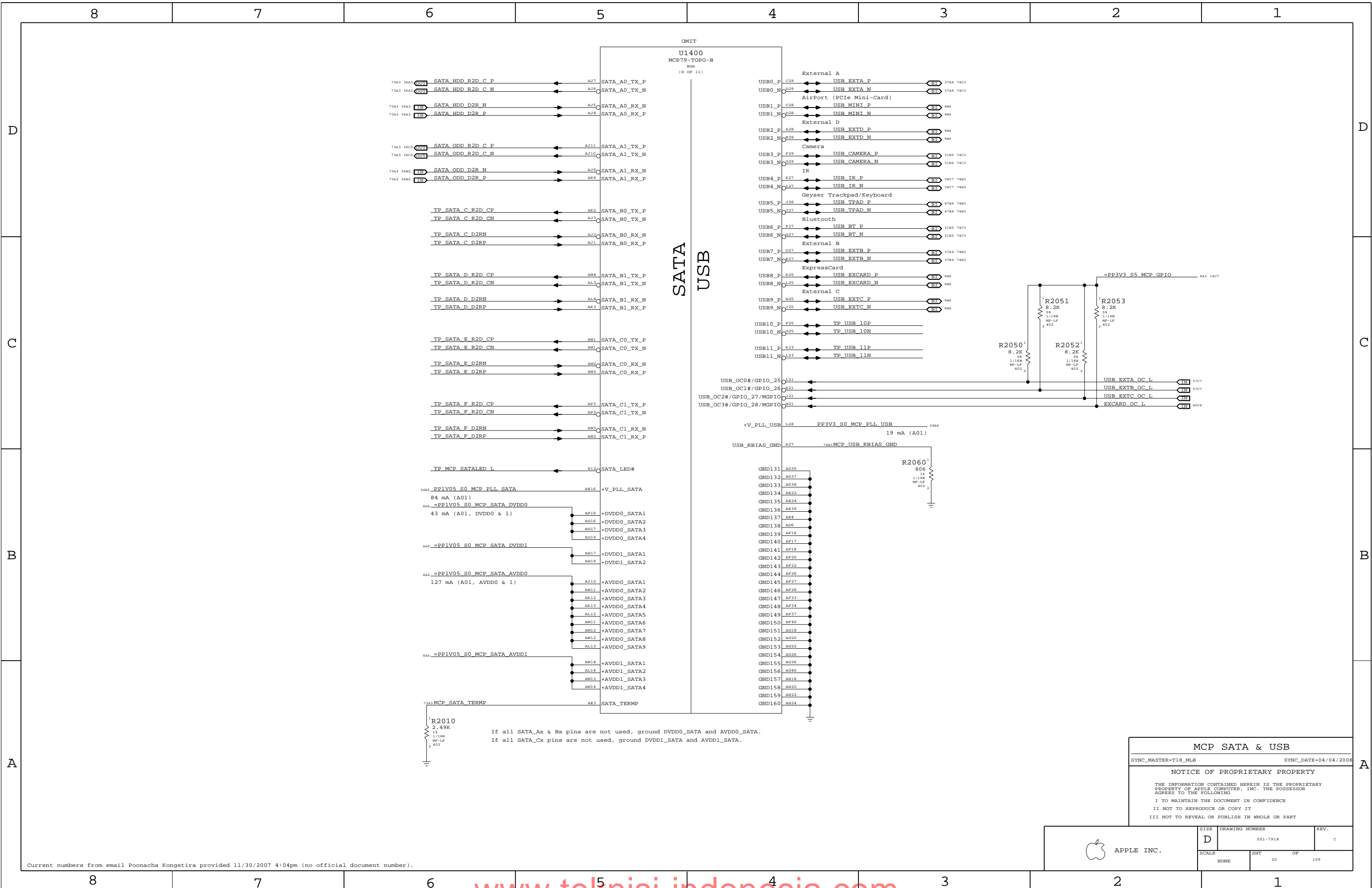
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APPLE INC.

SIZE D DRAWING NUMBER 051-7918 REV. C

SCALE NONE SHT 18 OF 109





Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP SATA & USB

SYNC\_MASTER=T18\_MLB

SYNC\_DATE=04/04/2008

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MCP79 A01 Silicon Support

SYNC\_MASTER=T18\_MLB

SYNC\_DATE=03/08/2008

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SCALE  
NONE

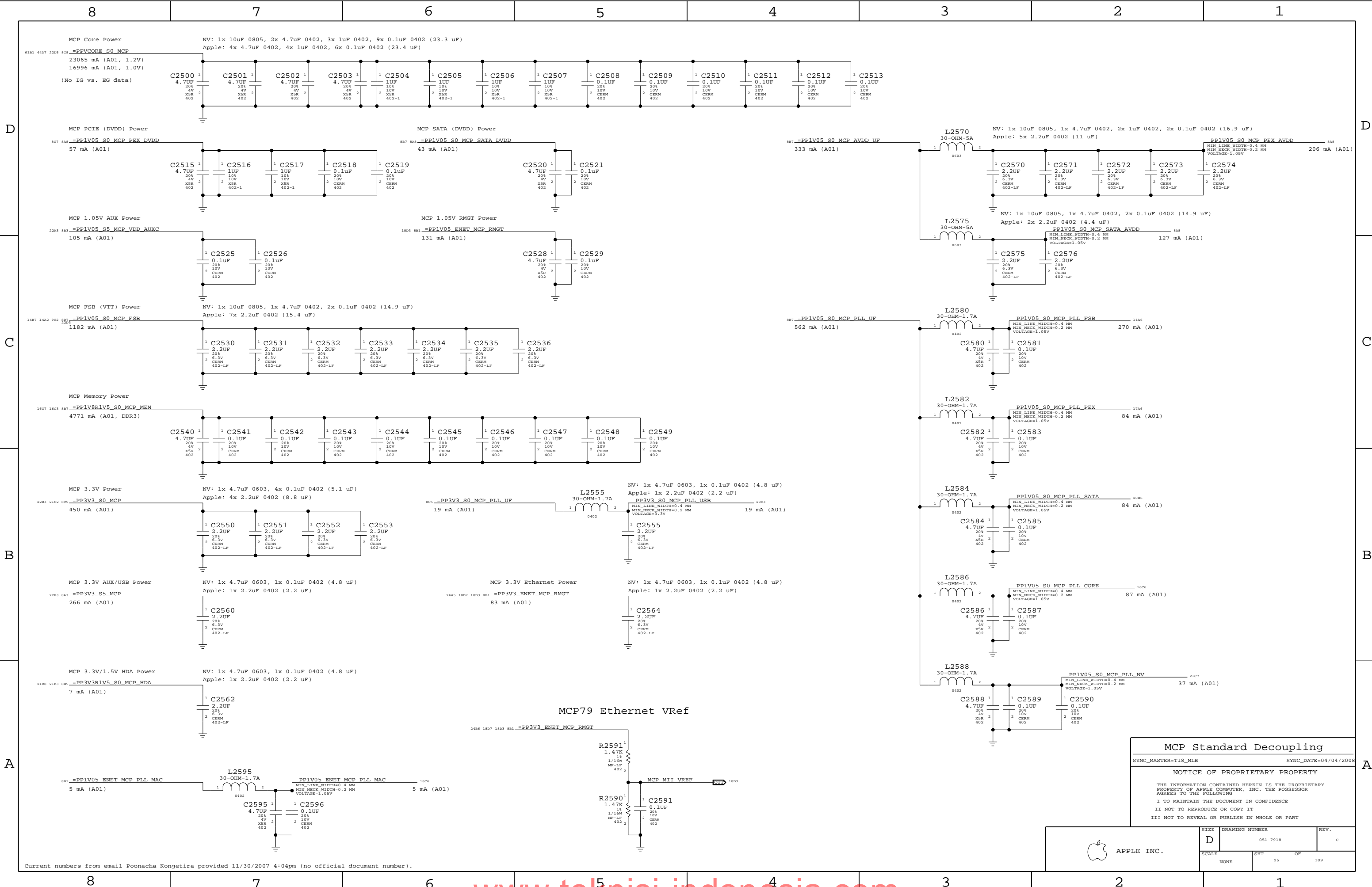
SIZE  
D

DRAWING NUMBER  
051-7918

SHT  
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REV.  
C

OF  
109



MCP Standard Decoupling

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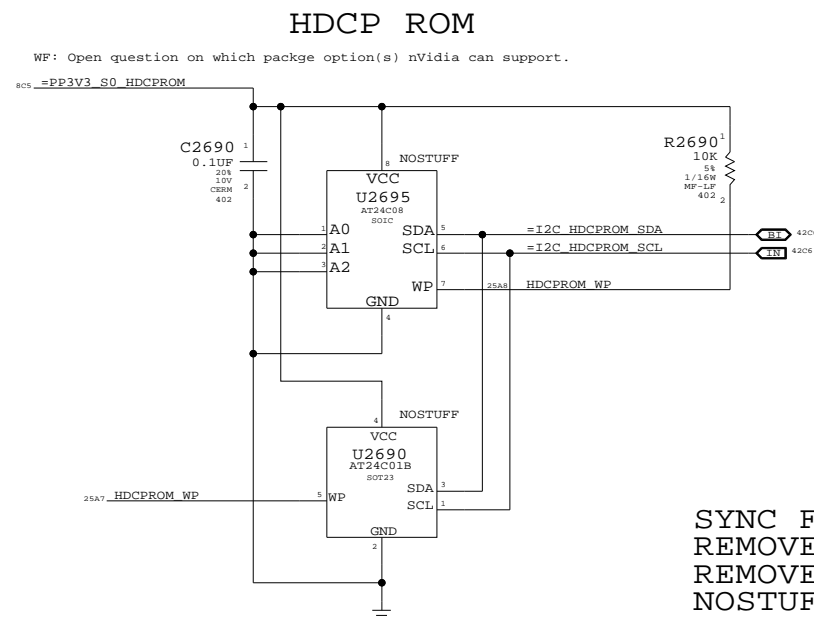
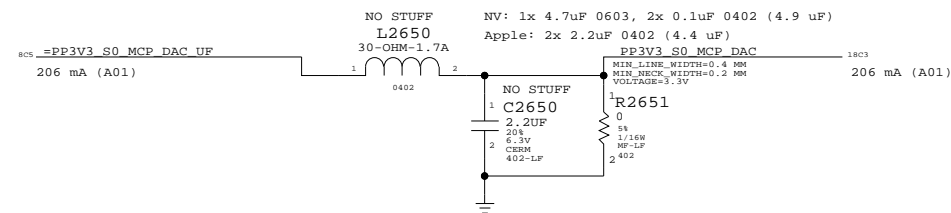
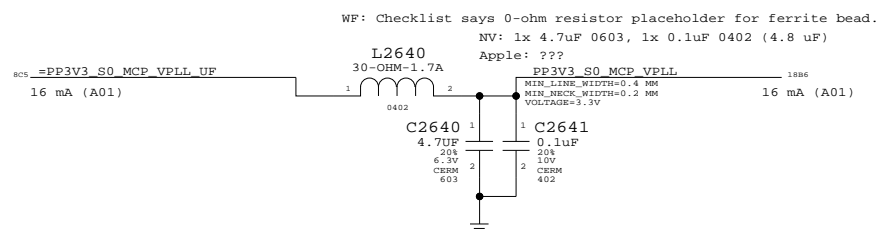
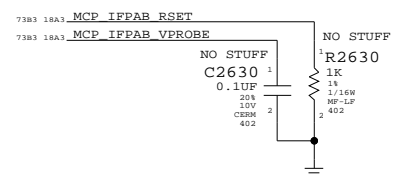
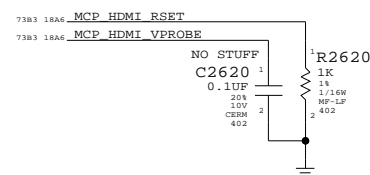
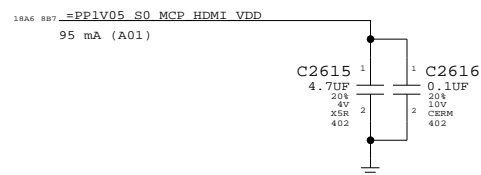
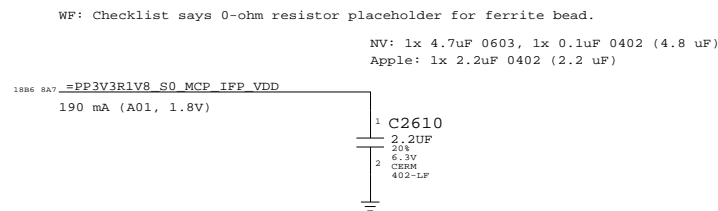
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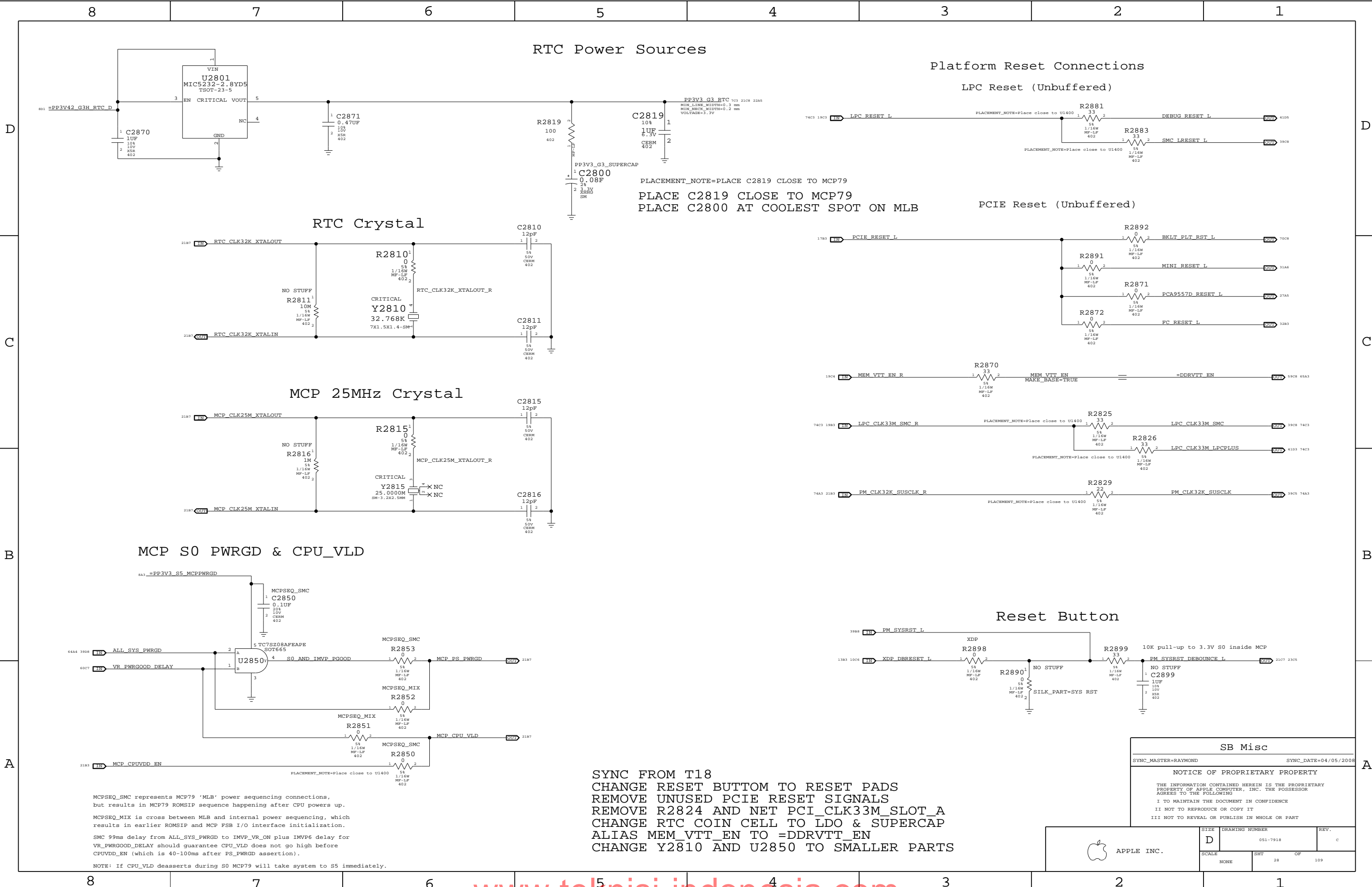
SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	25	109



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SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC

```



SYNC FROM T18  
CHANGE RESET BUTTON TO RESET PADS  
REMOVE UNUSED PCIE RESET SIGNALS  
REMOVE R2824 AND NET PCI\_CLK33M\_SLOT\_A  
CHANGE RTC COIN CELL TO LDO & SUPERCAP  
ALIAS MEM\_VTT\_EN TO =DDRVTT\_EN  
CHANGE Y2810 AND U2850 TO SMALLER PARTS

## Page Notes

Power aliases required by this page:

- =PP3V3\_S3\_VREFMRGN  
- =PP3V3\_S5\_VREFMRGN  
- =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:

- =I2C\_VREFDACS\_SCL  
- =I2C\_VREFDACS\_SDA  
- =I2C\_PCA9557D\_SCL  
- =I2C\_PCA9557D\_SDA

BOM options provided by this page:

VREFMRGN  
NO\_VREFMRGN

DAC channel  
Min DAC code  
Max DAC code  
Max sink I  
Max source I  
Nominal Vref  
Min Vref  
Max Vref  
Vref Stepping  
(per DAC LSB)

MEM A VREF DQ  
A  
0x00  
0x87  
-3.75 mA  
5 mA  
0.75 V  
0.375 V  
1.250 V  
6.5 mV

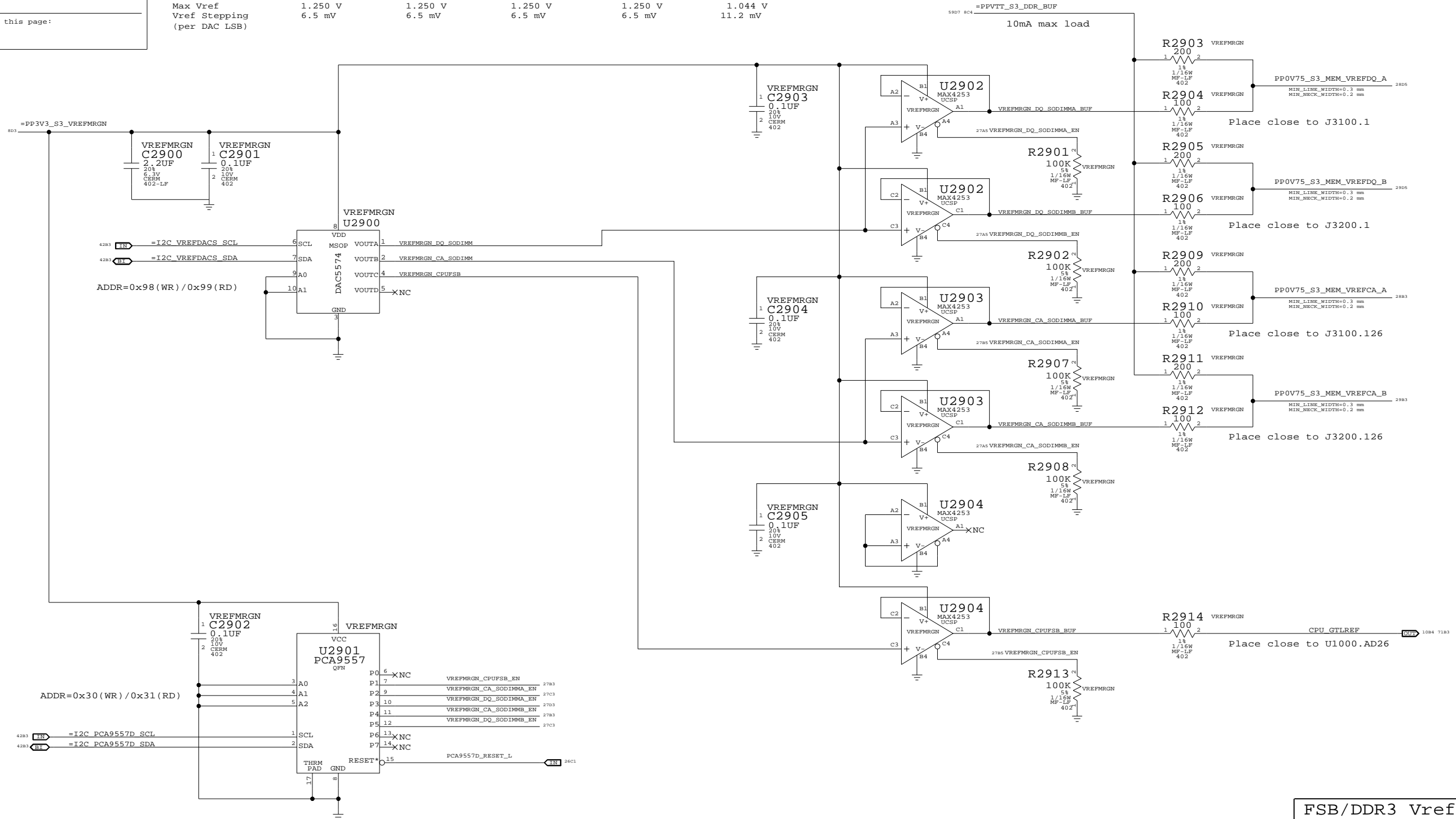
MEM A VREF CA  
B  
0x00  
0x87  
-3.75 mA  
5 mA  
0.75 V  
0.375 V  
1.250 V  
6.5 mV

MEM B VREF DQ  
A  
0x00  
0x87  
-3.75 mA  
5 mA  
0.75 V  
0.375 V  
1.250 V  
6.5 mV

MEM B VREF CA  
B  
0x00  
0x87  
-3.75 mA  
5 mA  
0.75 V  
0.375 V  
1.250 V  
6.5 mV

CPU FSB VREF  
C  
0x00  
0x55  
-0.91 mA  
0.52 mA  
0.70 V  
0.091 V  
1.044 V  
11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately  
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

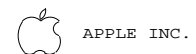
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

## FSB/DDR3 Vref Margining

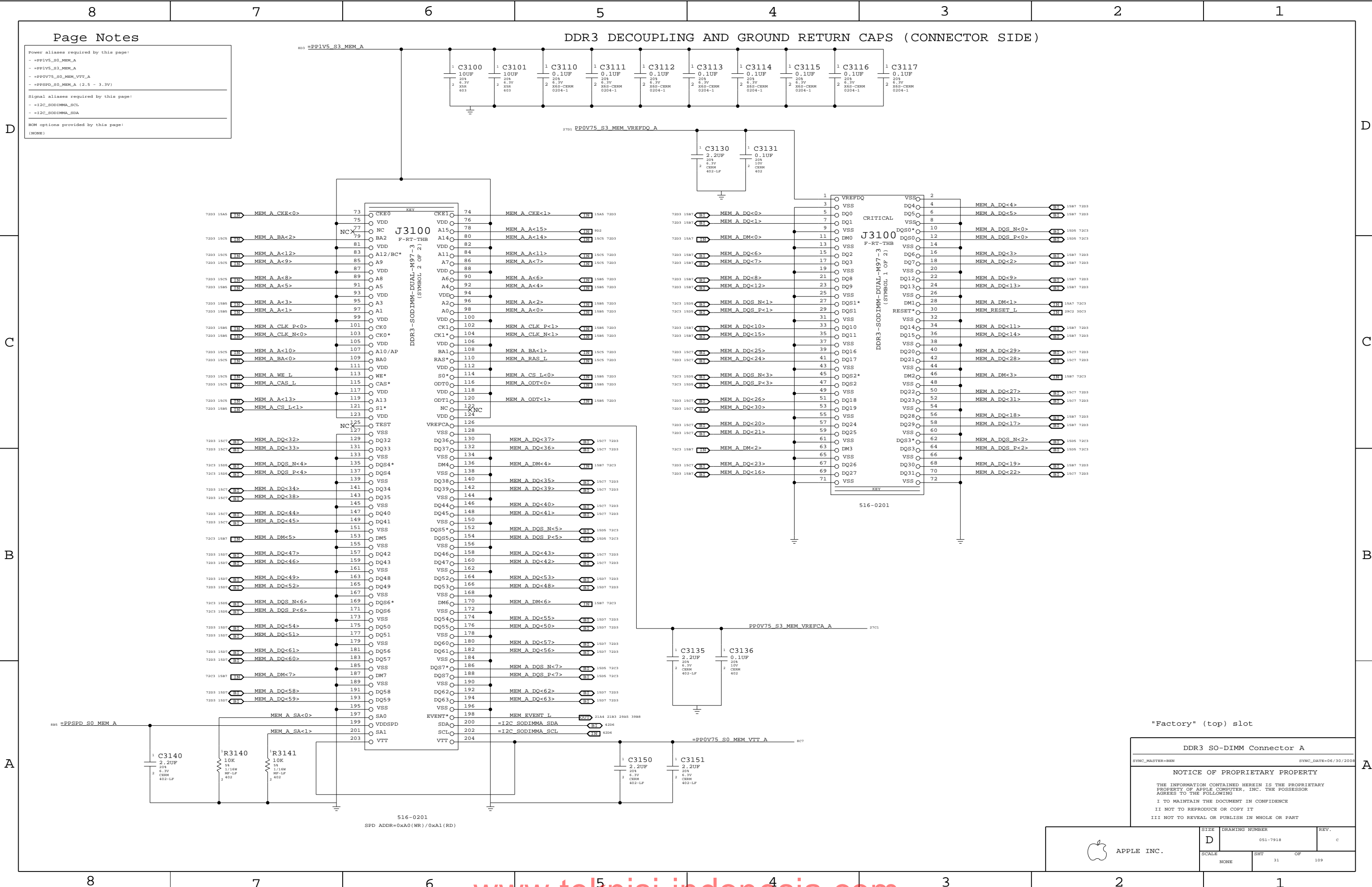
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SCALE	SHT	OF
NONE	29	109



Page Notes

Power aliases required by this page:

- =PP1V5\_S0\_MEM\_A
- =PP1V5\_S3\_MEM\_A
- =PP0V75\_S0\_MEM\_VTT\_A
- =PPSPD\_S0\_MEM\_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C\_SODIMMA\_SCL
- =I2C\_SODIMMA\_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC\_MASTER=BBN SYNC\_DATE=06/30/2008

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	D	051-7918	C
SCALE	SHT		
	NONE 31 OF 109		

## Page Notes

Power aliases required by this page:

- =PP1V5\_S0\_MEM\_B  
- =PP1V5\_S3\_MEM\_B  
- =PP0V75\_S0\_MEM\_VTT\_B  
- =PPSPD\_S0\_MEM\_B (2.5 - 3.3V)

Signal aliases required by this page:

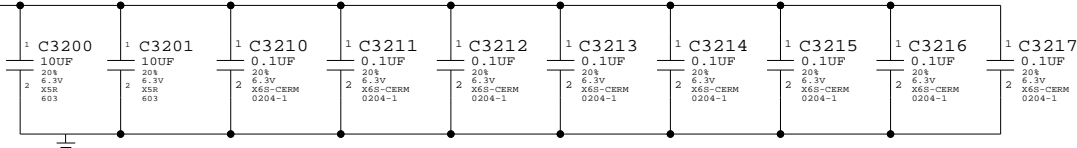
- =I2C\_SODIMMB\_SCL  
- =I2C\_SODIMMB\_SDA

BOM options provided by this page:

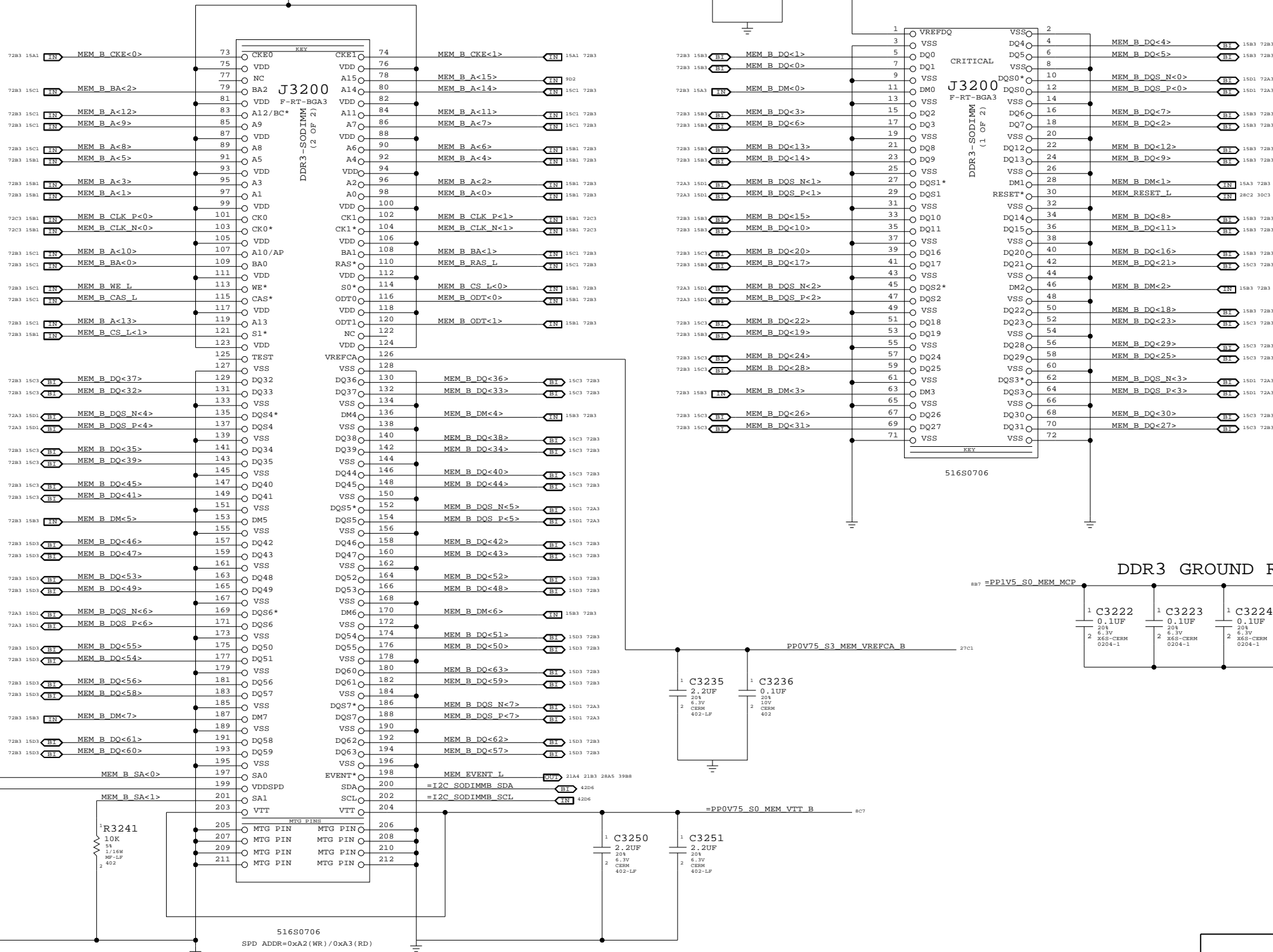
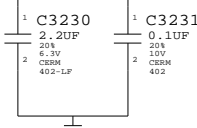
(NONE)

## DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

803 =PP1V5\_S3\_MEM\_B

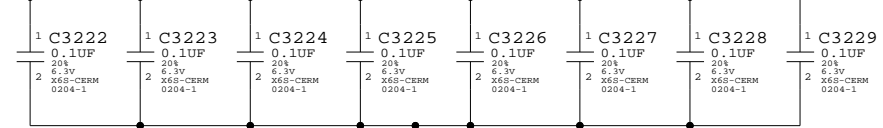


2701 PP0V75\_S3\_MEM\_VREFDQ\_B

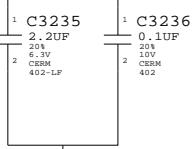


## DDR3 GROUND RETURN CAPS (MCP SIDE)

887 =PP1V5\_S0\_MEM\_MCP



PP0V75\_S3\_MEM\_VREFCA\_B



807

=PP0V75\_S0\_MEM\_VTT\_B

807

"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

SYNC\_MASTER=BBN SYNC\_DATE=05/09/2008

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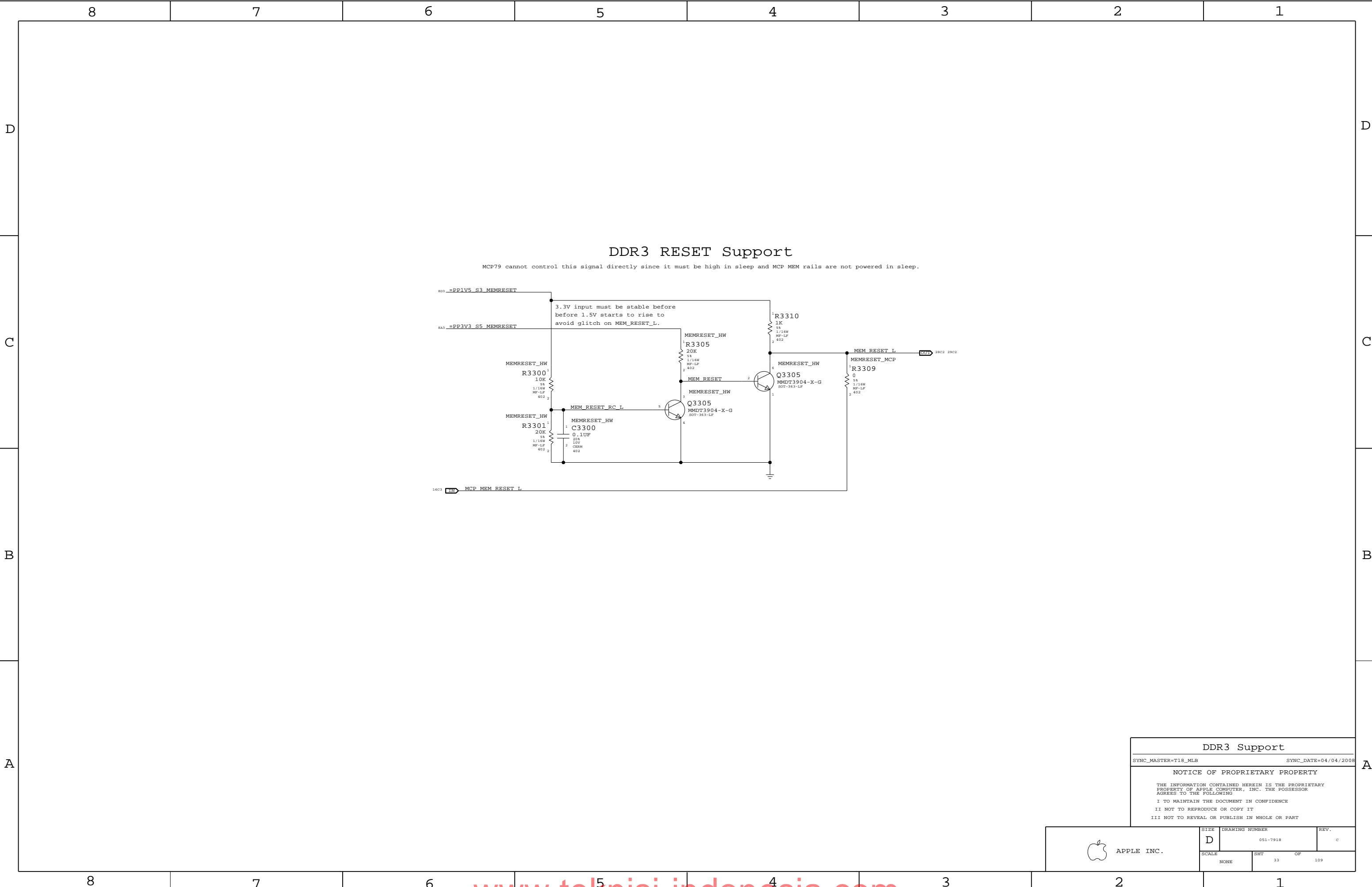
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

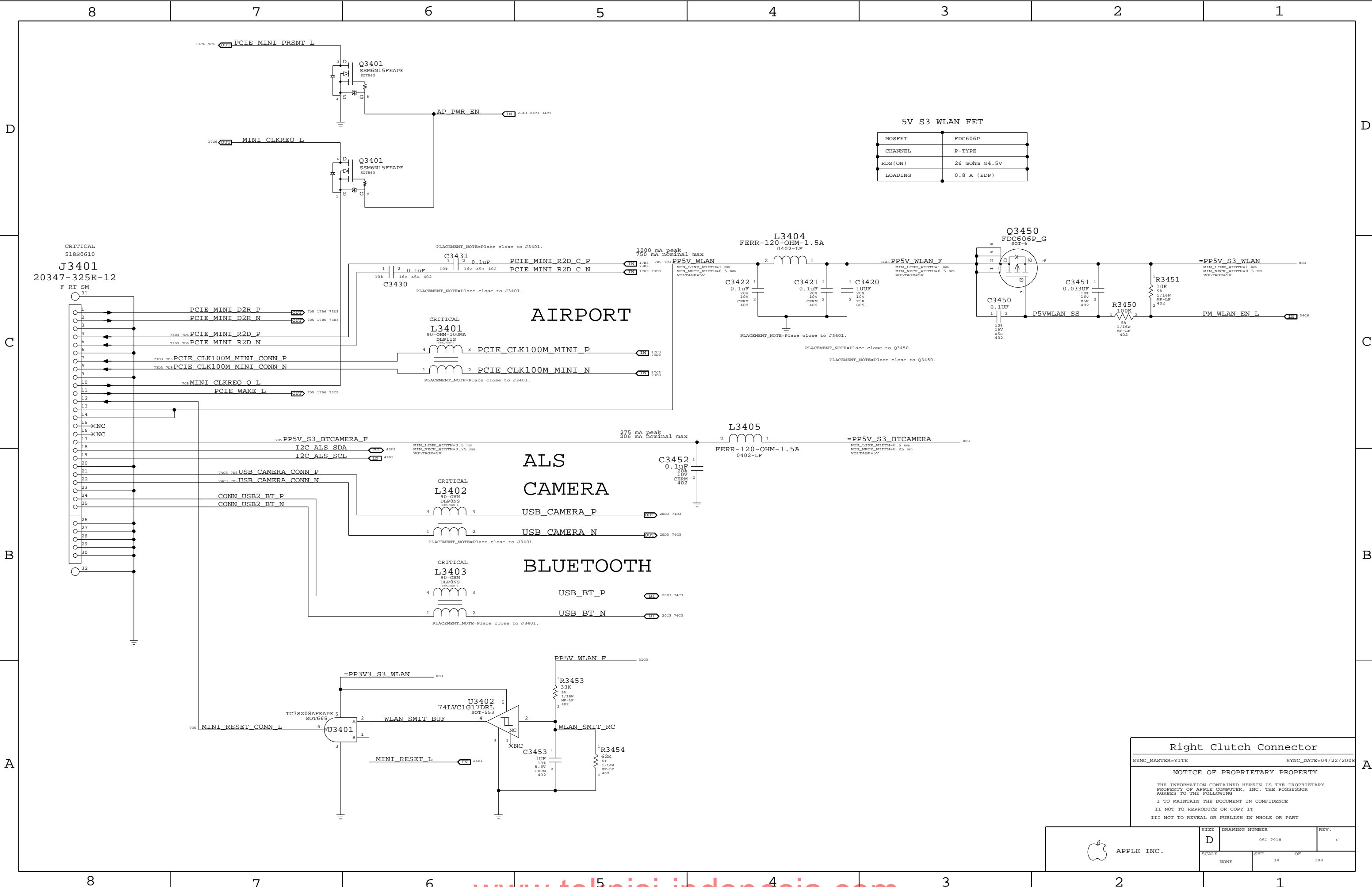


APPLE INC.

SIZE D DRAWING NUMBER 051-7918 REV. C

SCALE NONE SHT 32 OF 109





5V S3 WLAN FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

Right Clutch Connector

SYNC\_MASTER=YITE

SYNC\_DATE=04/22/2008

NOTICE OF PROPRIETARY PROPERTY

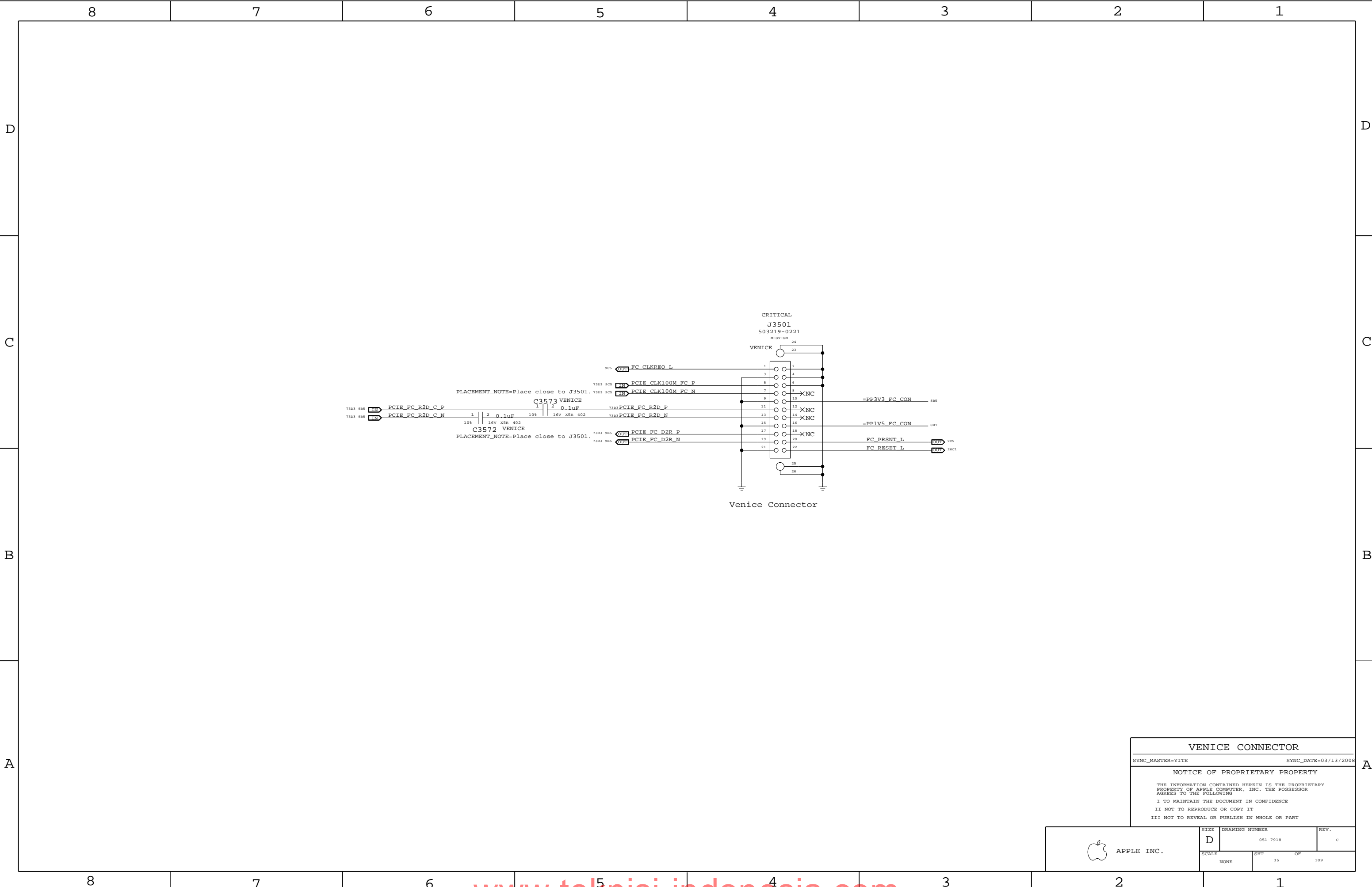
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	D	051-7918	c
SCALE		SHT	OF
NONE		34	109



VENICE CONNECTOR			
SYNC_MASTER=YITE		SYNC_DATE=03/13/2008	
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE	NONE	SHT	OF
		35	109

D

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B

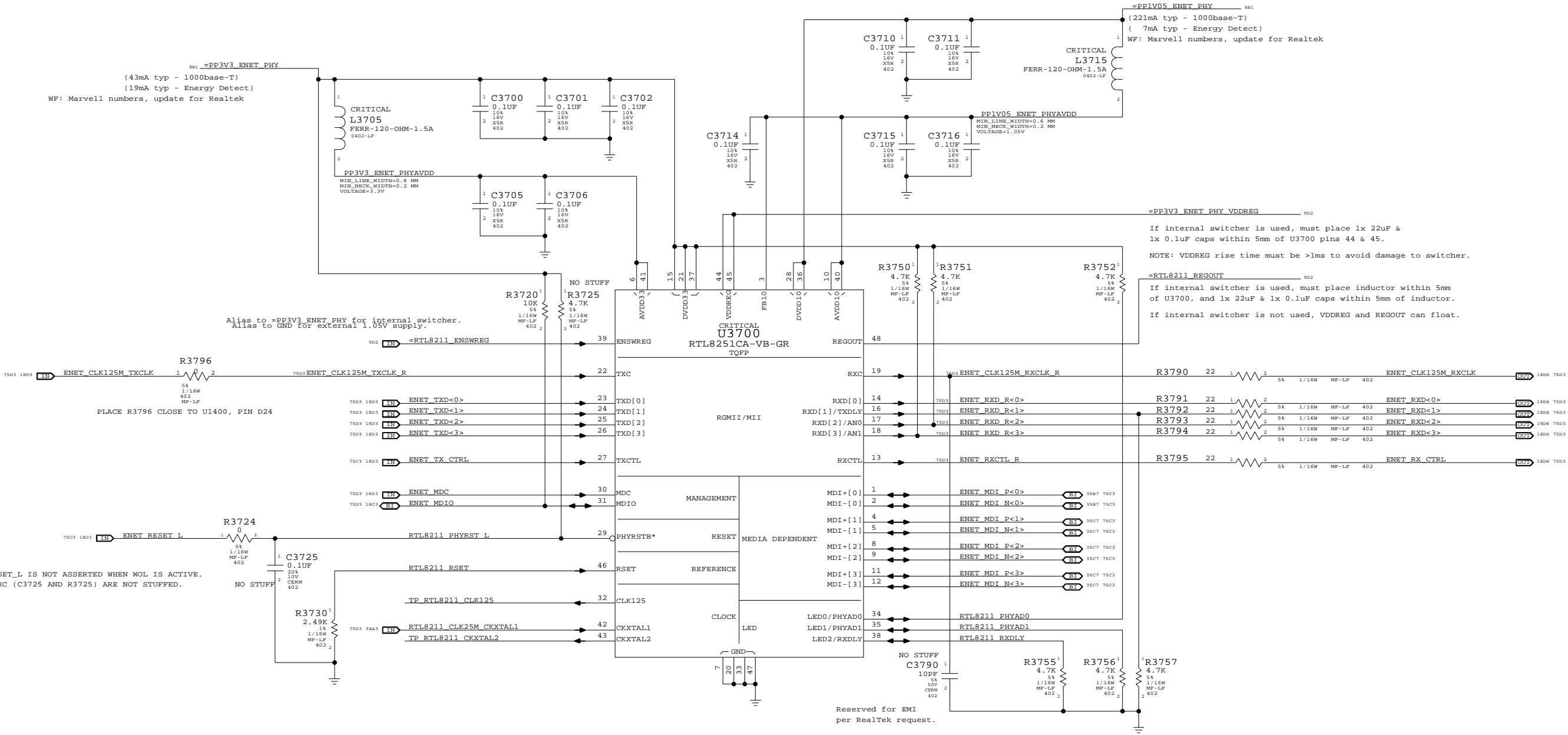
A

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A



Configuration Settings:

PHYAD = 01 (PHY Address 00001)  
AN[1:0] = 11 (Full auto-negotiation)  
RXDLY = 0 (RXCLK transitions with data)  
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC\_MASTER=SUMA

SYNC\_DATE=05/23/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7918

REV.

C

SCALE

NONE

SHT

37

OF

109

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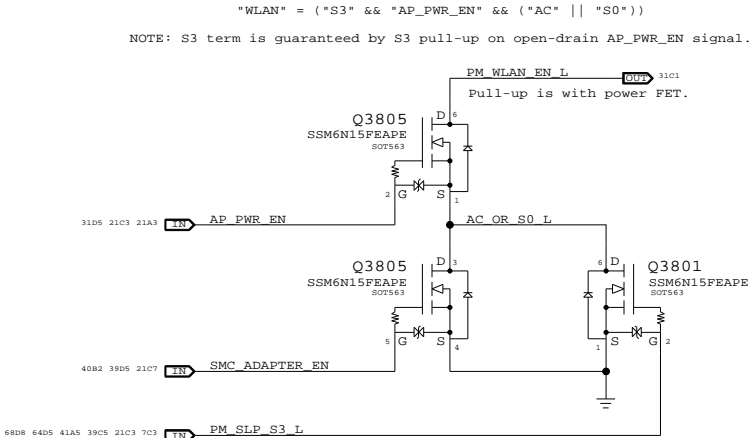
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C

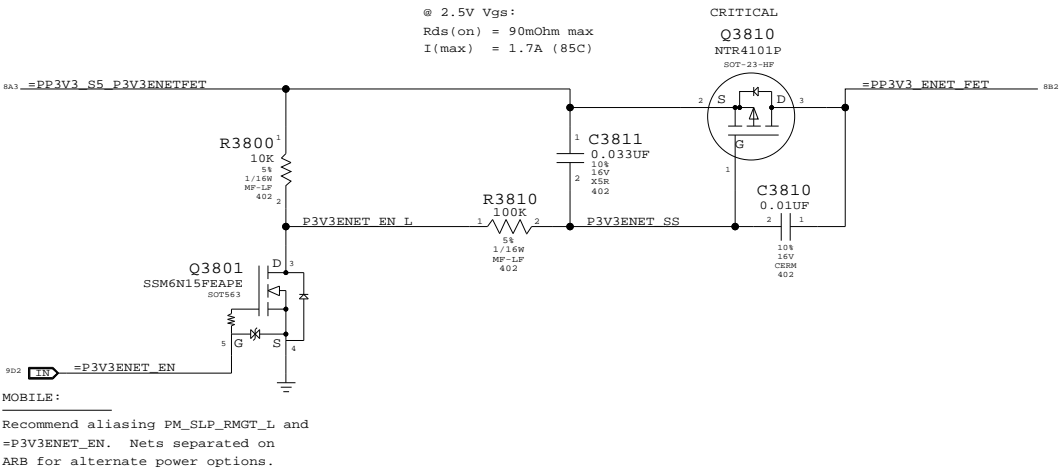
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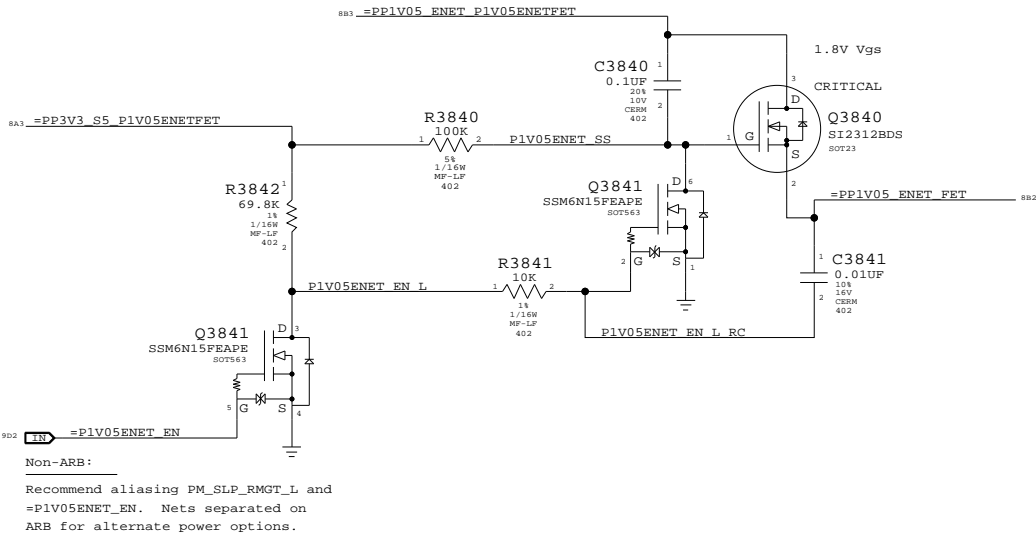
WLAN Enable Generation



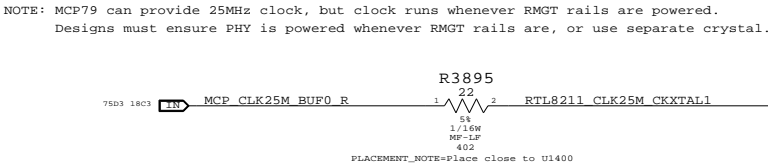
3.3V ENET FET



1.05V ENET FET

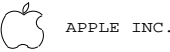


RTL8211 25MHz Clock




Ethernet & AirPort Support

SYNC_MASTER=SUMA		SYNC_DATE=07/01/2008	
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SIZE	DRAWING NUMBER	REV.
D	051-7918	c
SCALE	SHT	OF
NONE	38	109



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	D	051-7918		C
	SCALE	SHT		OF
	NONE	39		109

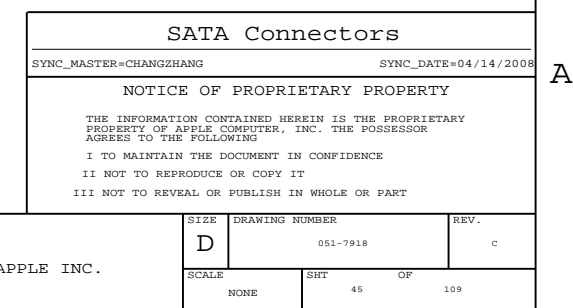
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## C

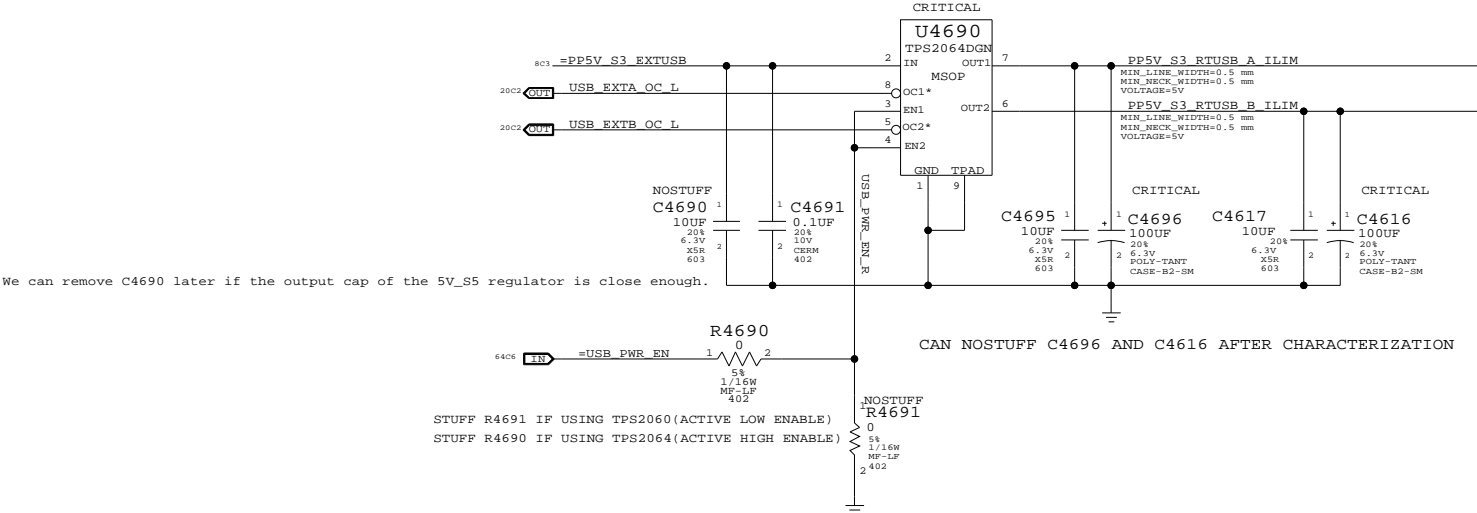


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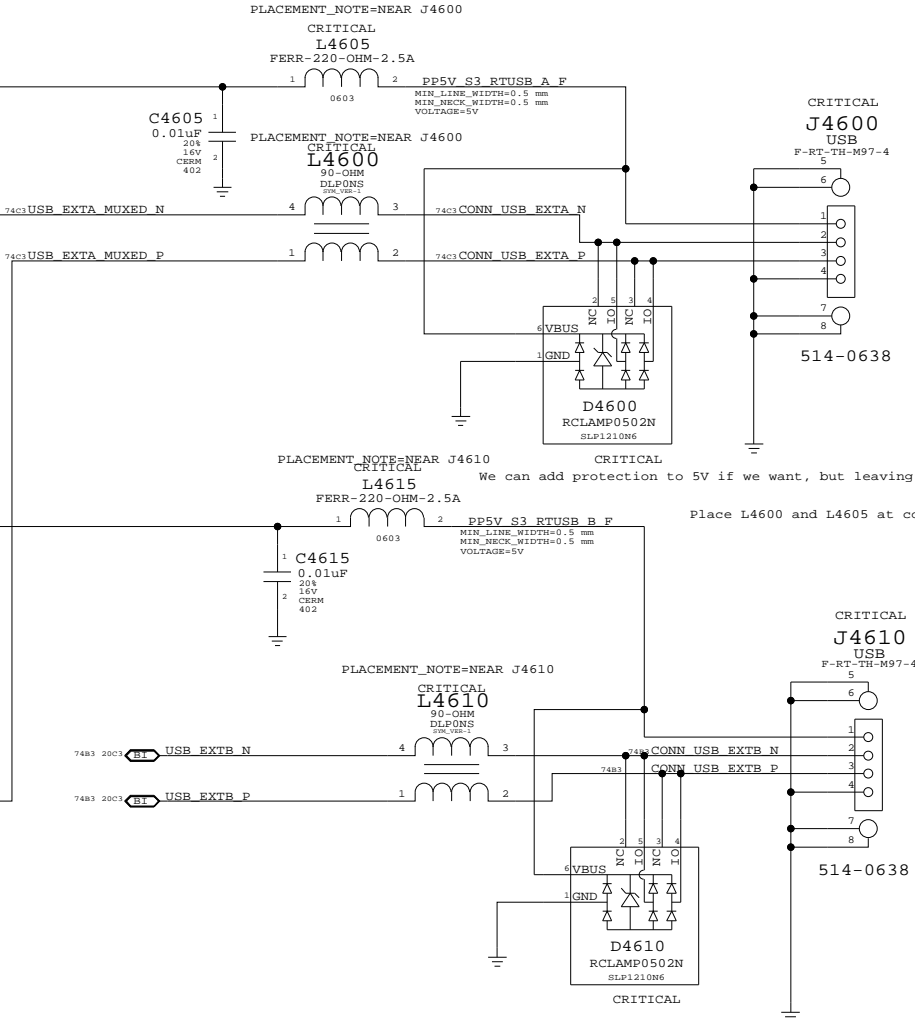
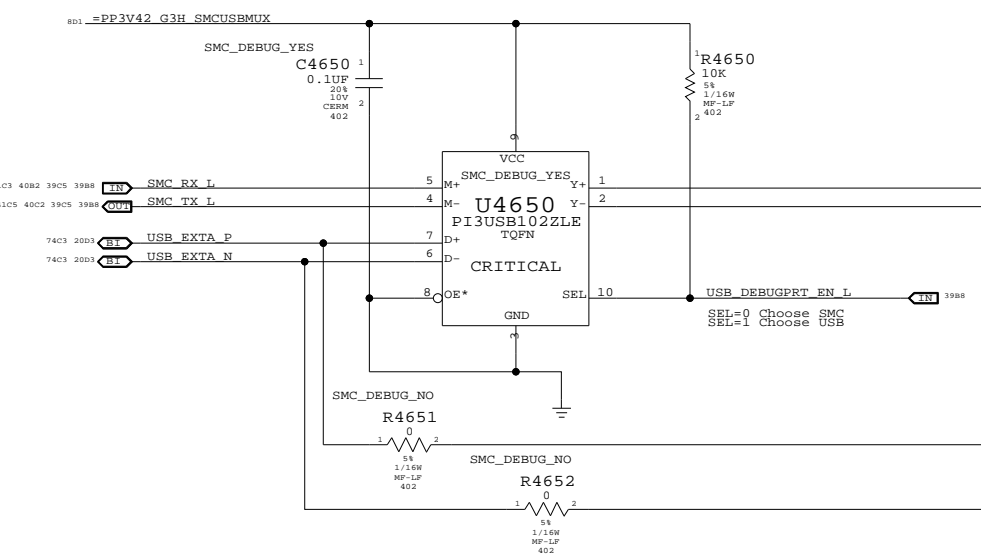


Port Power Switch

USB PORT A (FRONT PORT)



USB/SMC Debug Mux



USB PORT B (BACK PORT)

External USB Connectors		
SYNC_MASTER=YUAN.MA		SYNC_DATE=01/18/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	C
SCALE		SHT	OF
NONE		46	109

D

C

B

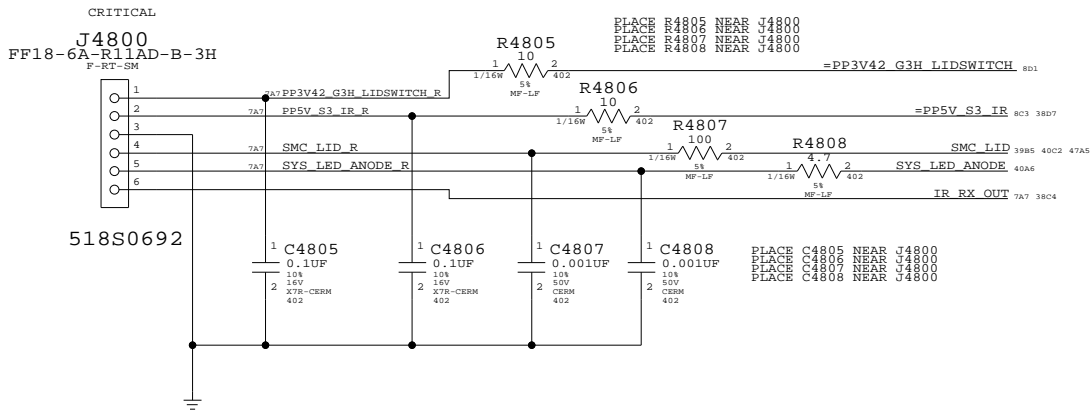
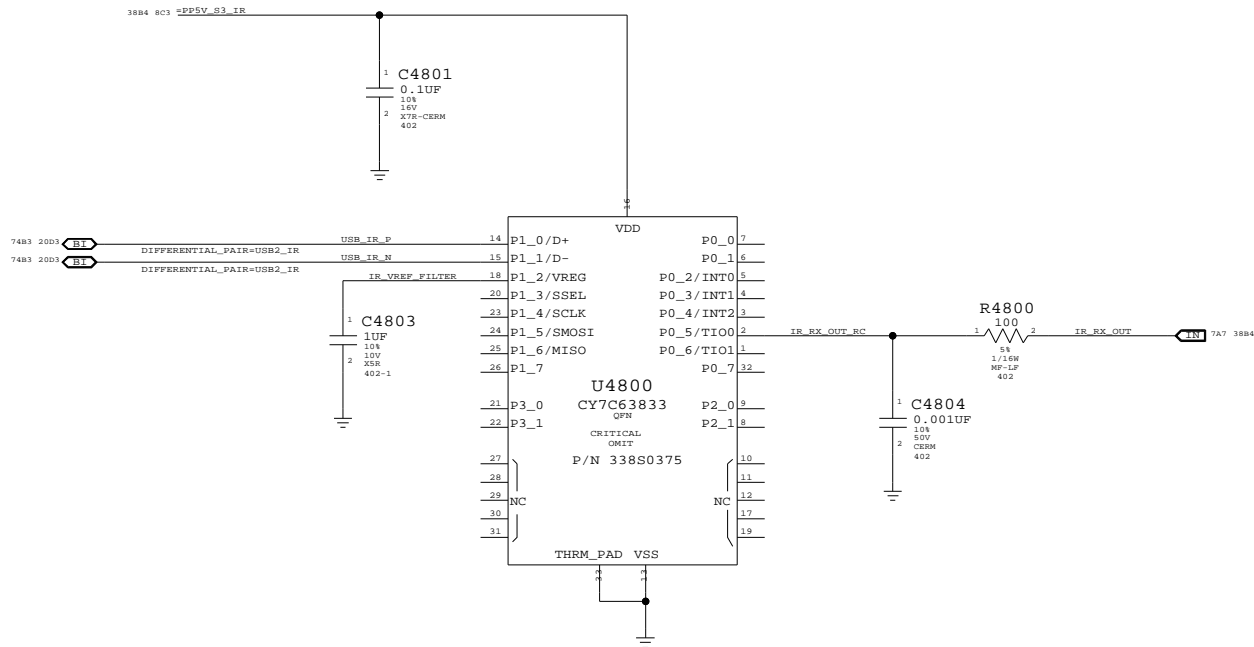
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A



# Front Flex Support

SYNC\_MASTER=YUAN.MA SYNC\_DATE=05/28/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7918

REV.

C

SCALE

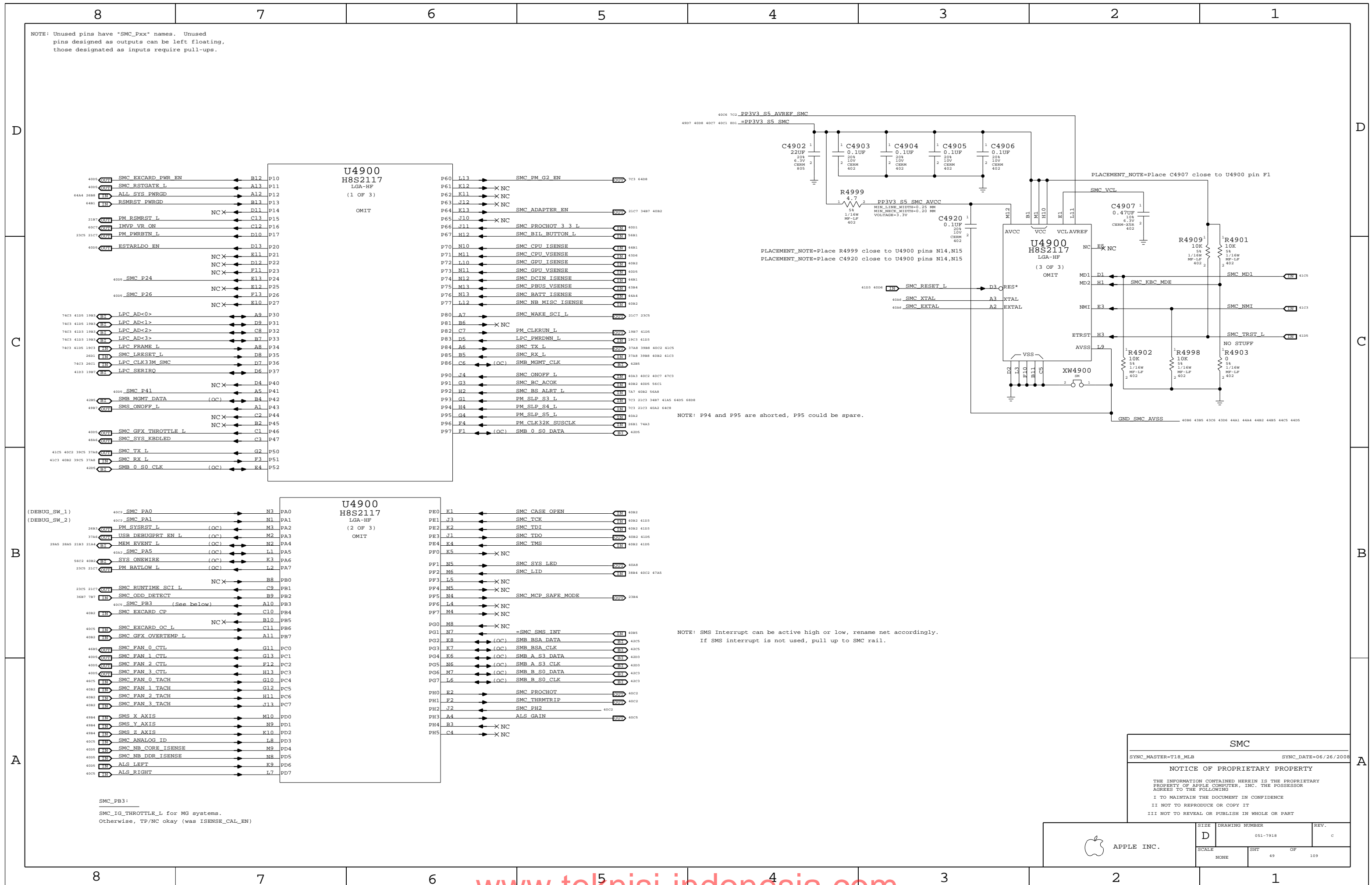
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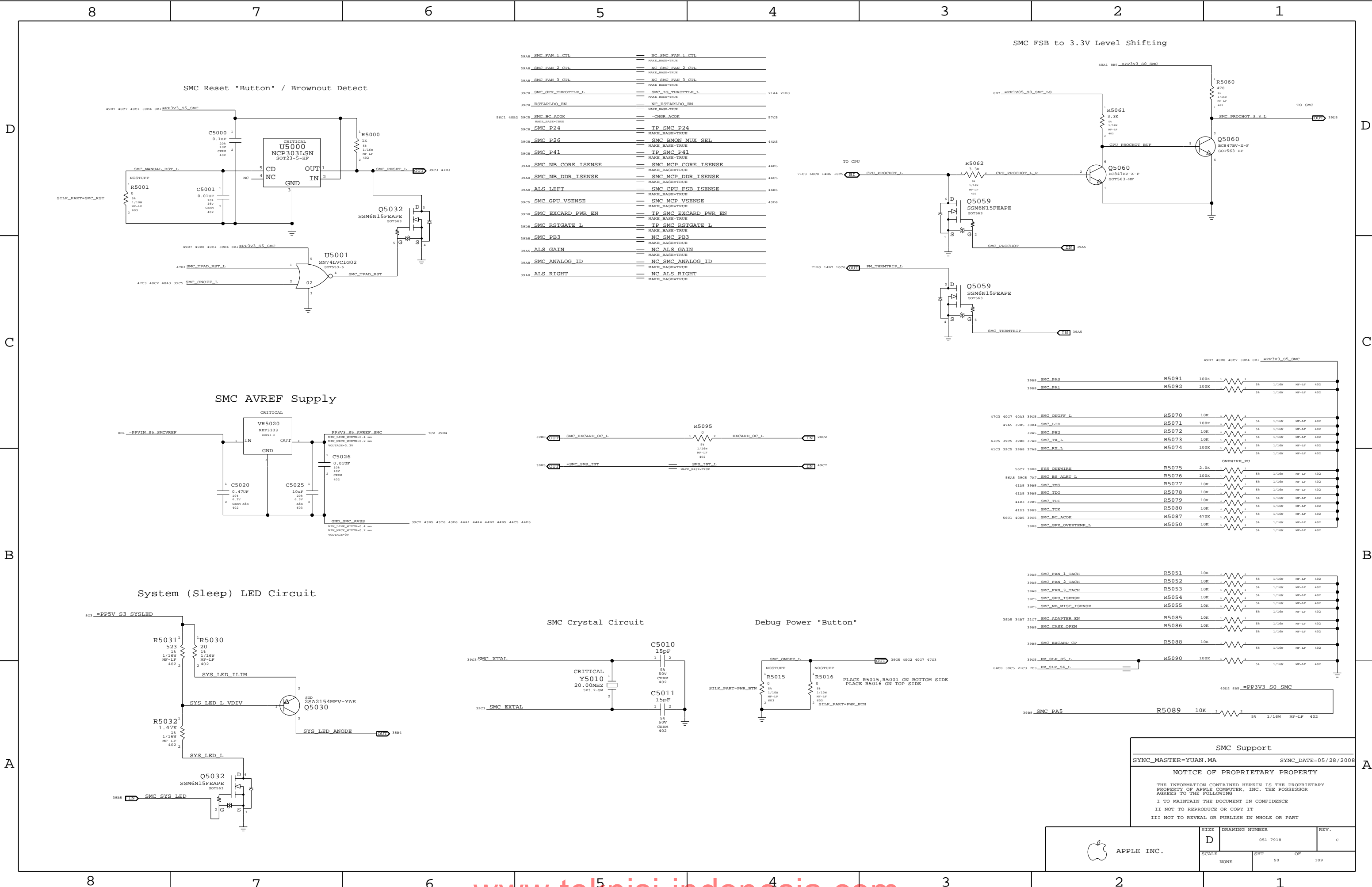
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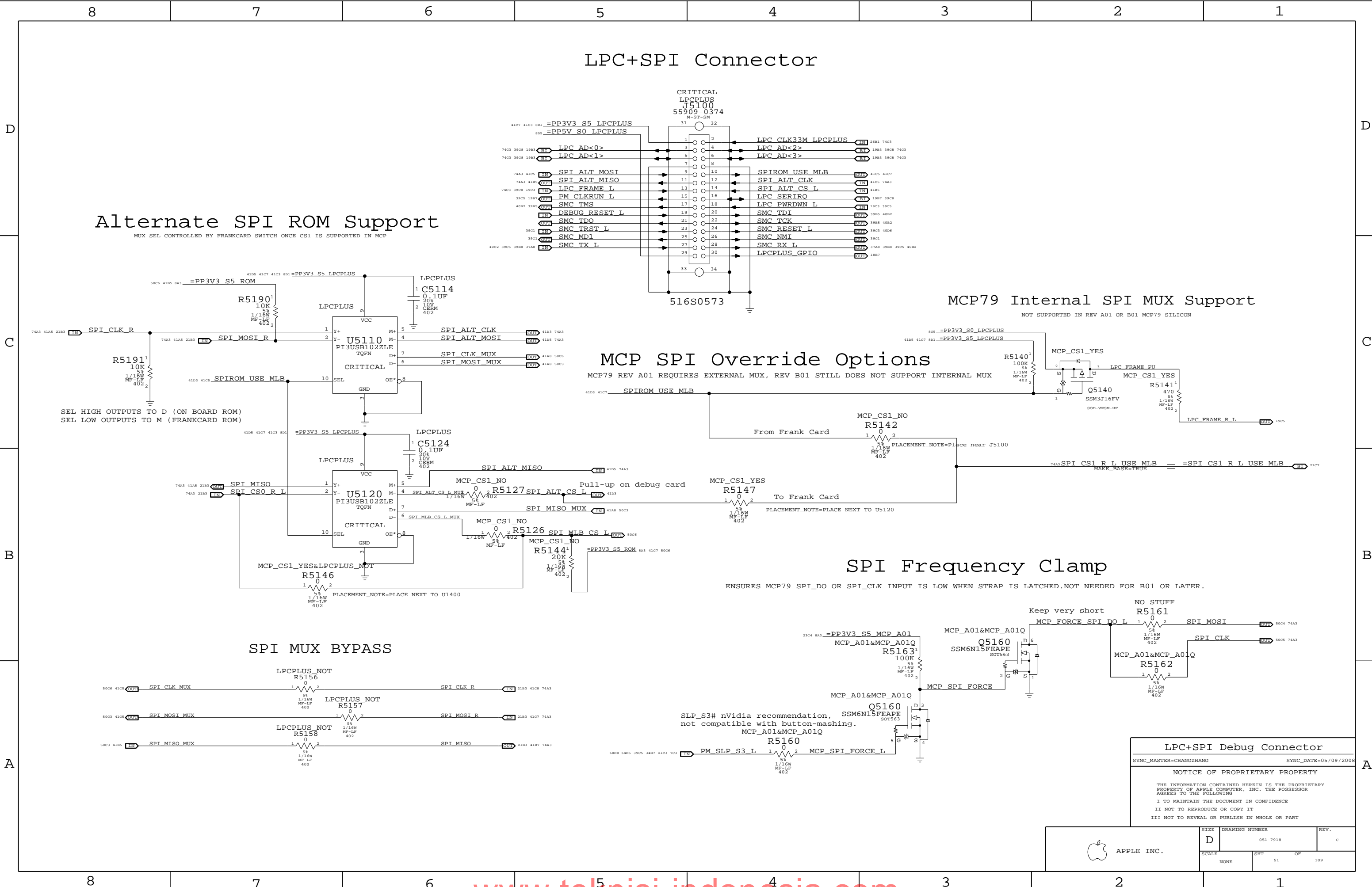
48

OF

109







LPC+SPI Connector

Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP

MCP79 Internal SPI MUX Support

NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX

SPI Frequency Clamp

ENSURES MCP79 SPI\_DO OR SPI\_CLK INPUT IS LOW WHEN STRAP IS LATCHED. NOT NEEDED FOR B01 OR LATER.

SPI MUX BYPASS

LPC+SPI Debug Connector

SYNC\_MASTER=CHANGZHANG SYNC\_DATE=05/09/2008

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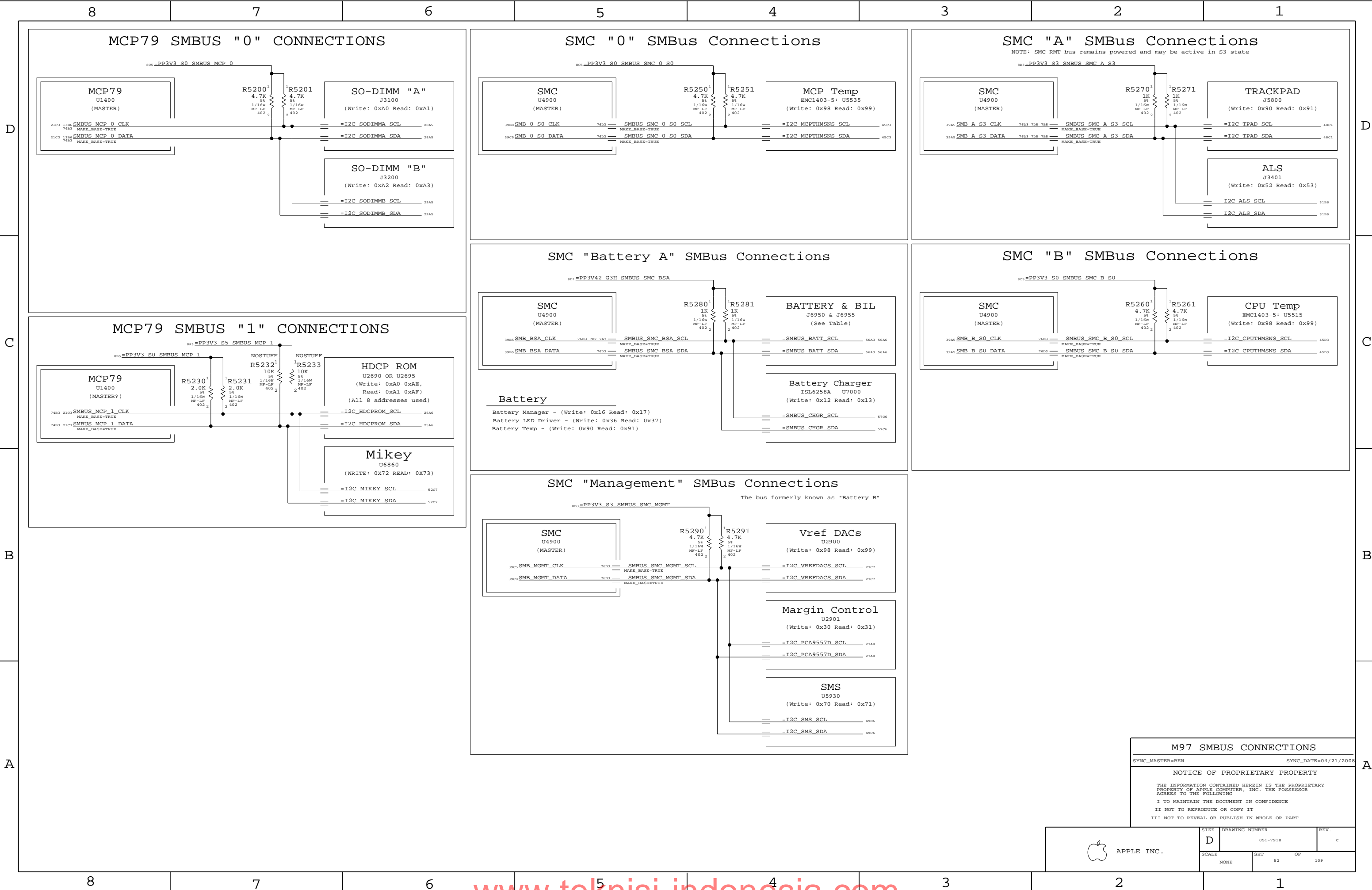
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APPLE INC.

SIZE	D	DRAWING NUMBER	051-7918	REV.	C
SCALE	NONE	SHT	51	OF	109



M97 SMBUS CONNECTIONS

SYNC\_MASTER=BEN SYNC\_DATE=04/21/2008

NOTICE OF PROPRIETARY PROPERTY

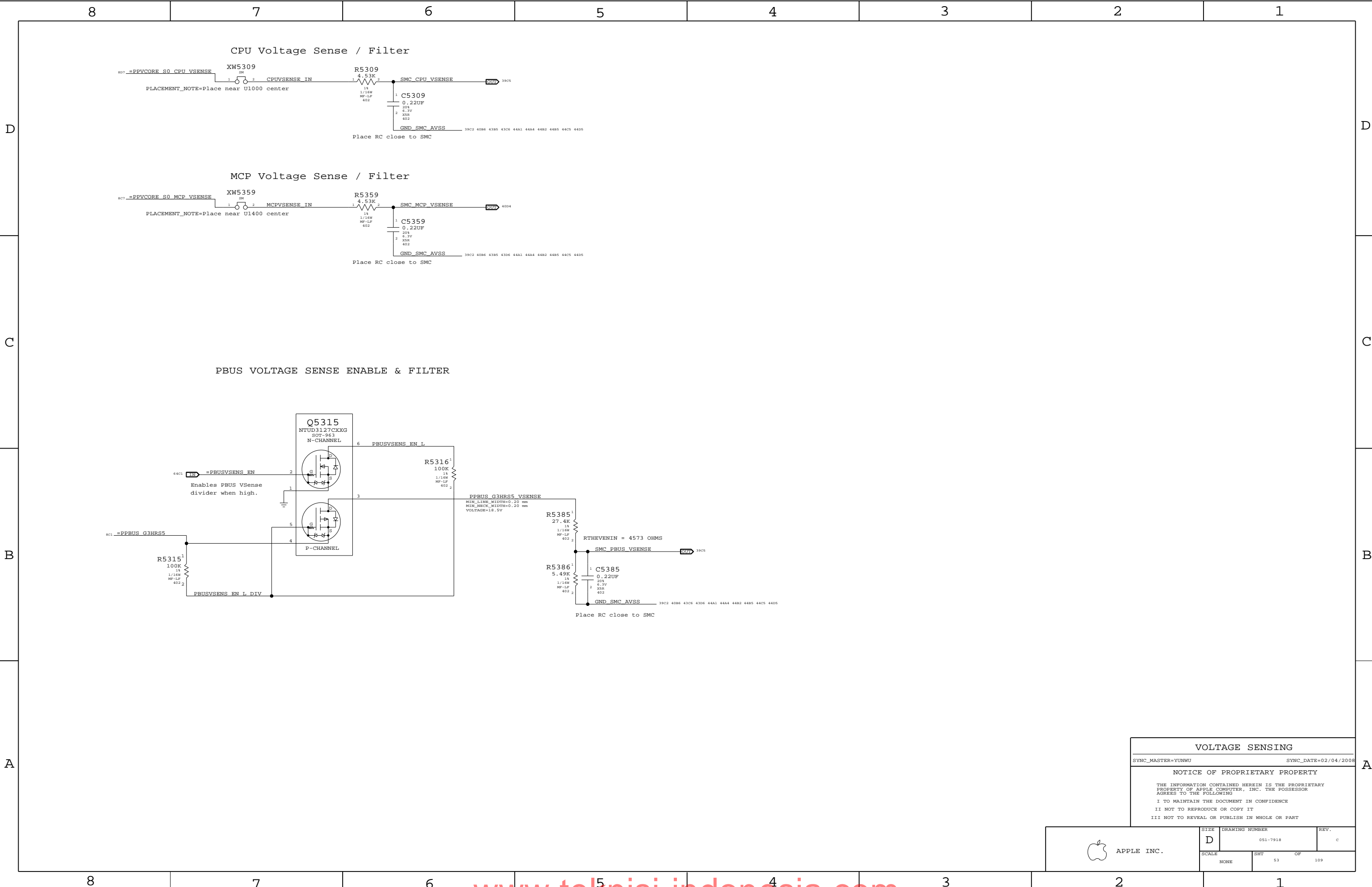
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE	NONE	SHT	OF
		52	109



VOLTAGE SENSING		
SYNC_MASTER=YUNWU		SYNC_DATE=02/04/2008
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
SIZE D	DRAWING NUMBER 051-7918	REV. c
	SCALE NONE	SHT 53
OF 109		





## D



## C

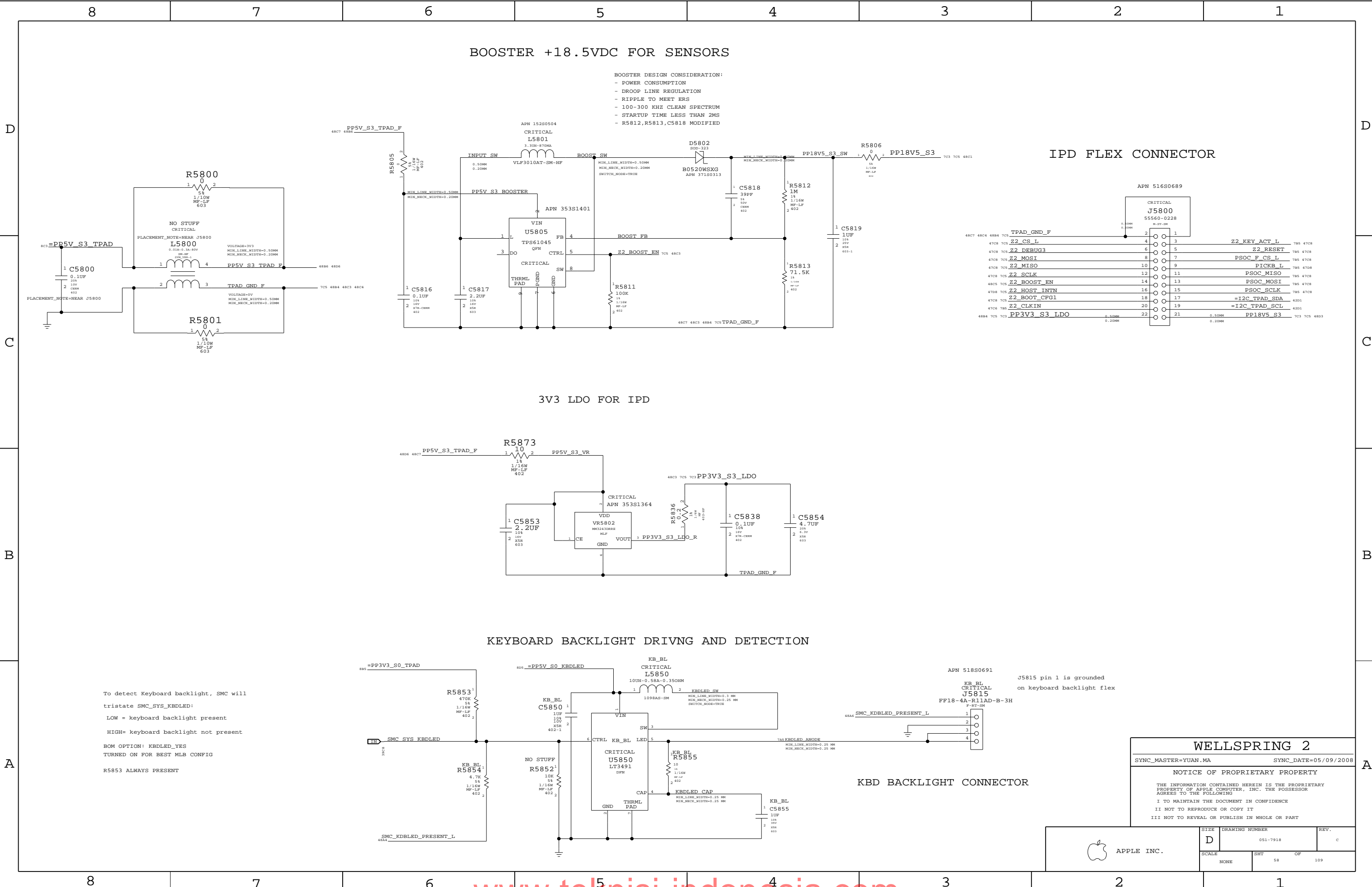


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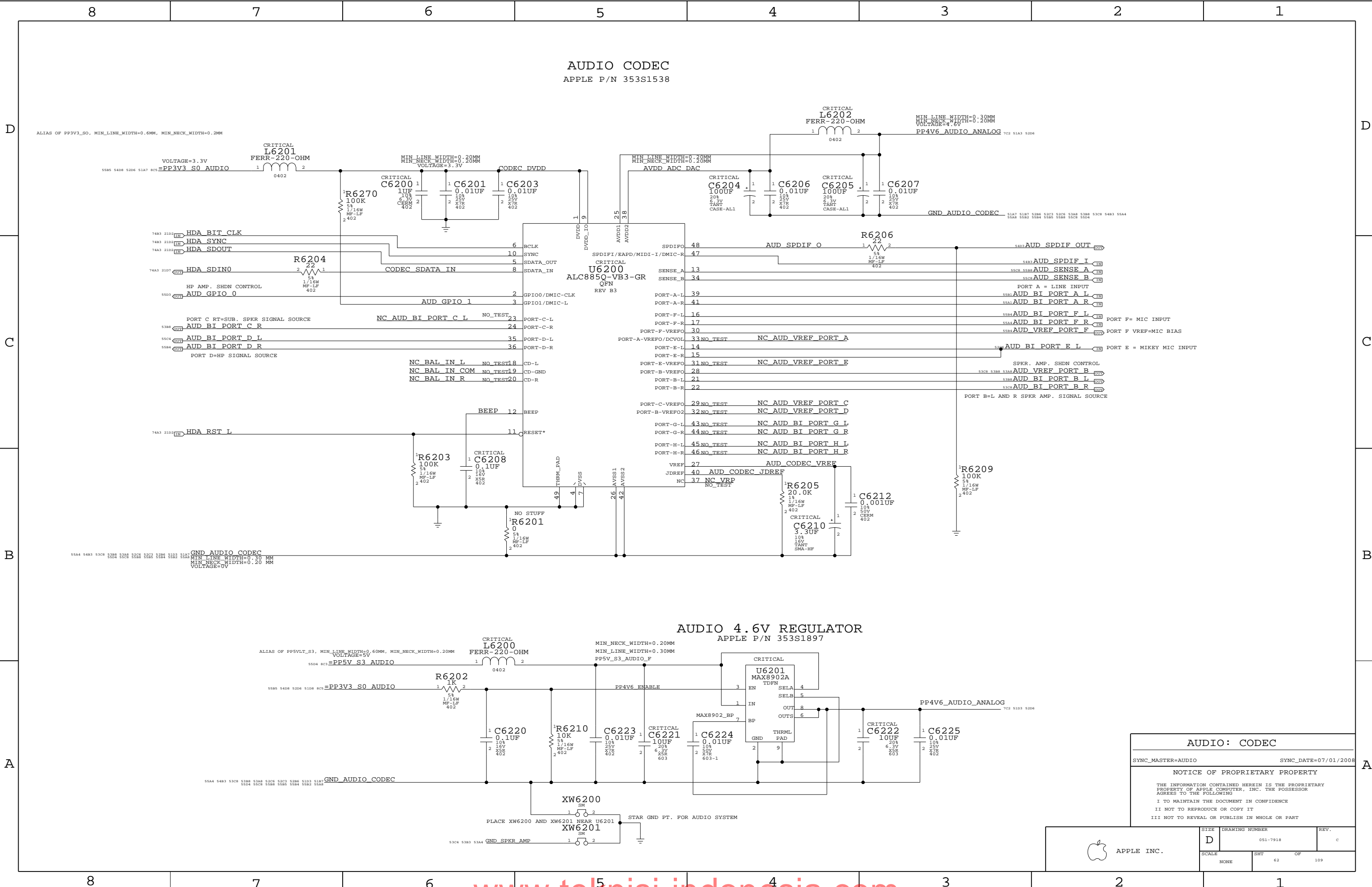


B



www.teknisi-indonesia.com





AUDIO: CODEC		
SYNC_MASTER=AUDIO		SYNC_DATE=07/01/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
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SCALE		SHT	OF
NONE		62	109

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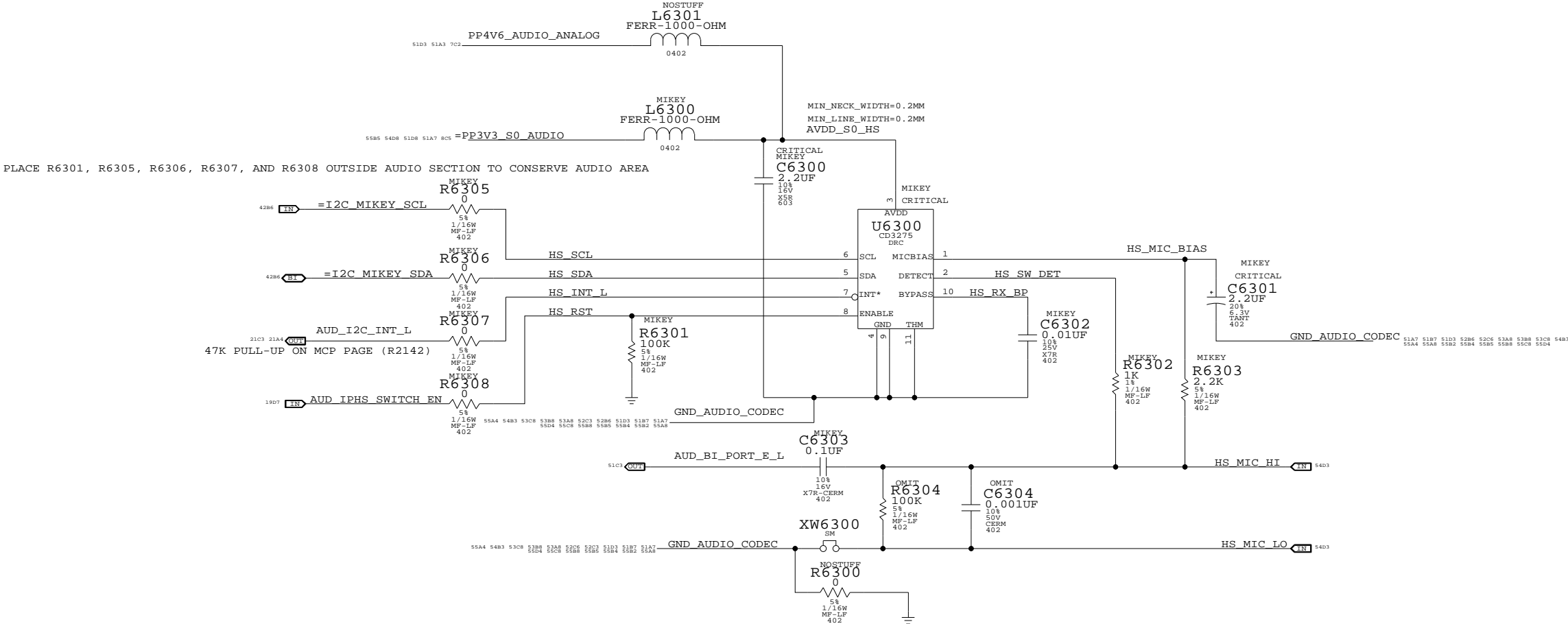
D

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# MIKEY RECEIVER CKT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0114	1	100K 5% 0402 RESISTOR	R6304	?	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	R6304	?	NOMIKEY
132S0045	1	0.001UF 50V 10% 0402 CAP	C6304	?	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6304	?	NOMIKEY

## AUDIO: MIKEY

SYNC\_MASTER=AUDIO SYNC\_DATE=07/03/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7918

REV.

C

SCALE

NONE

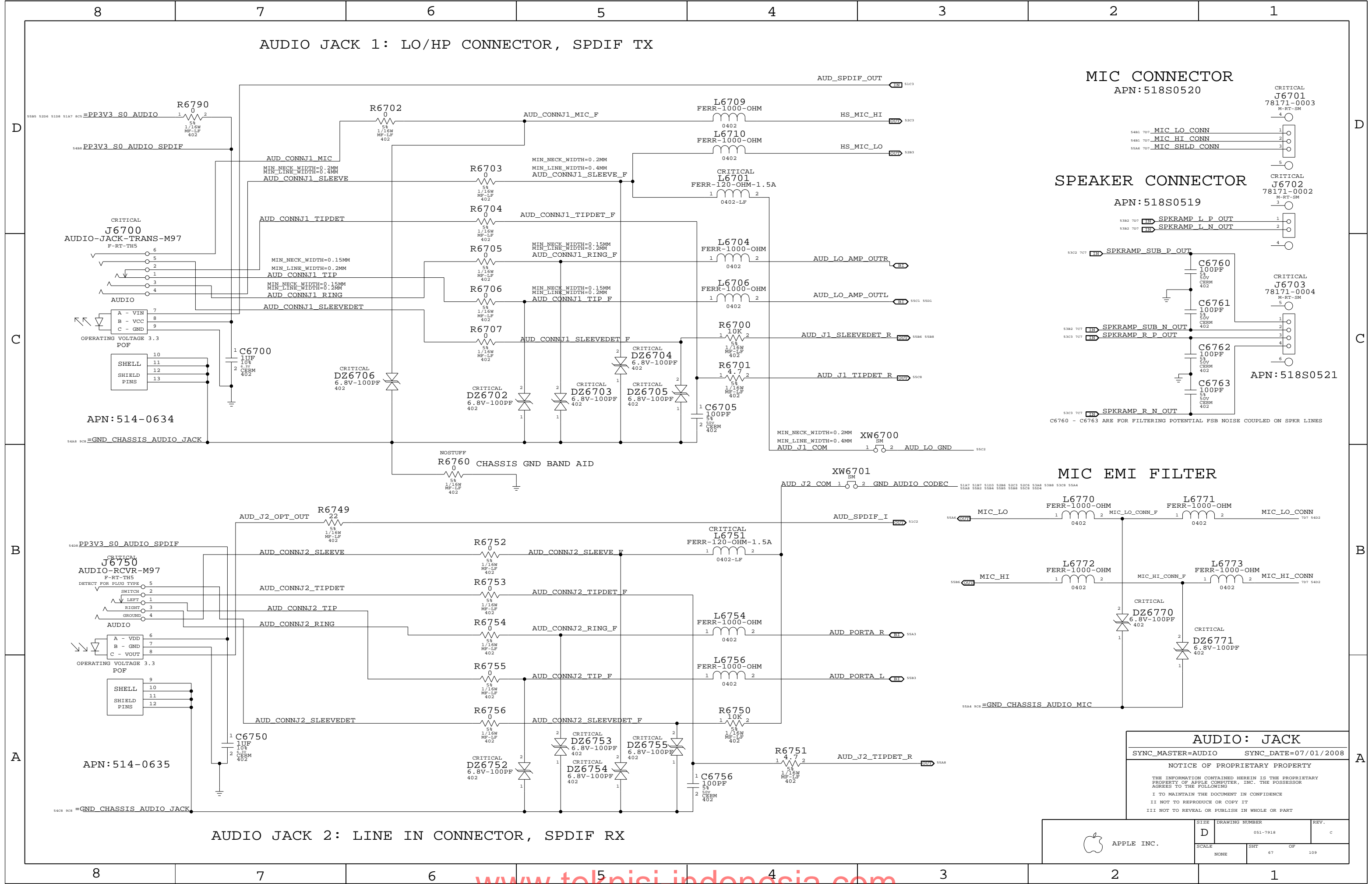
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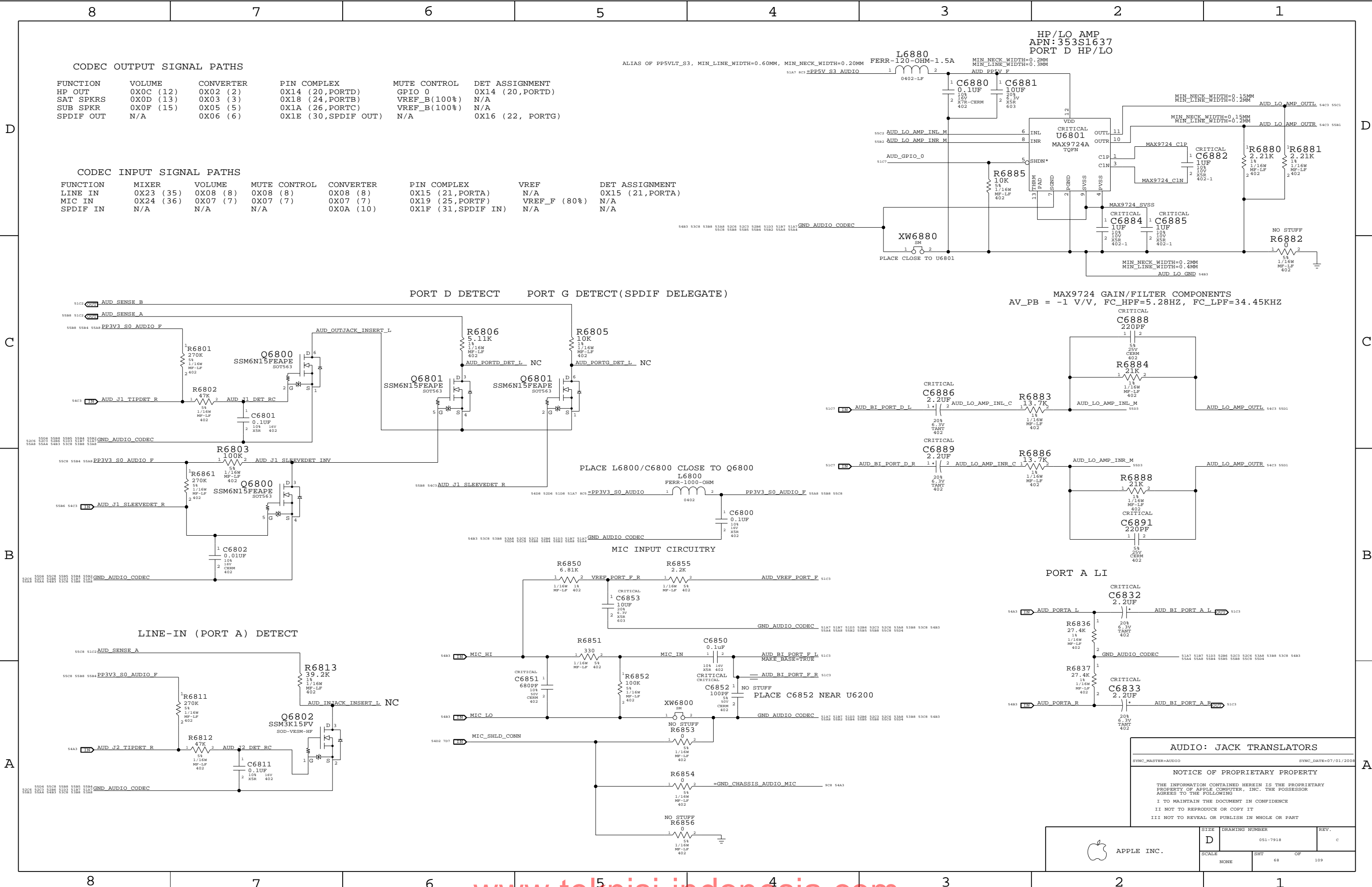
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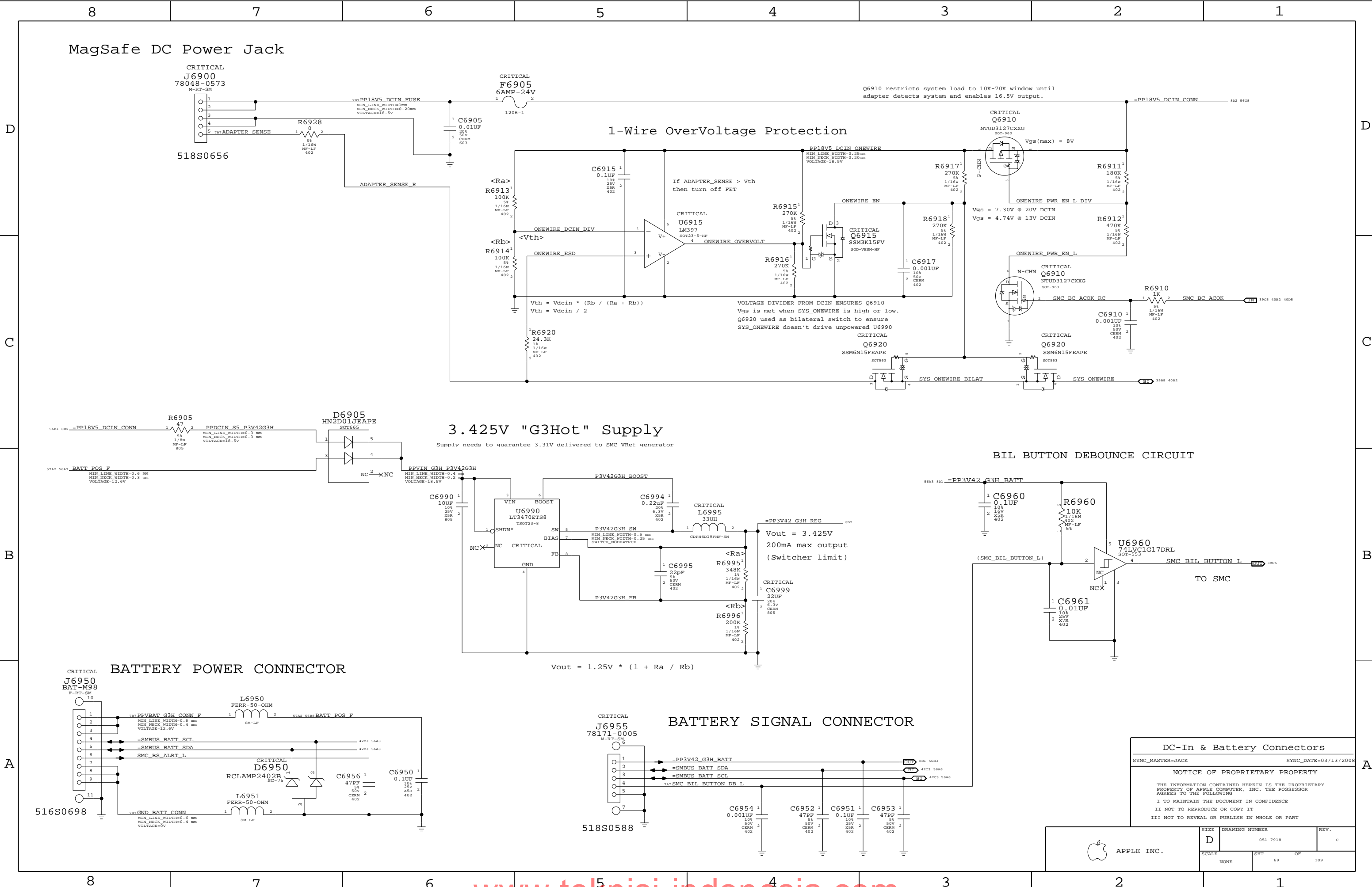
OF

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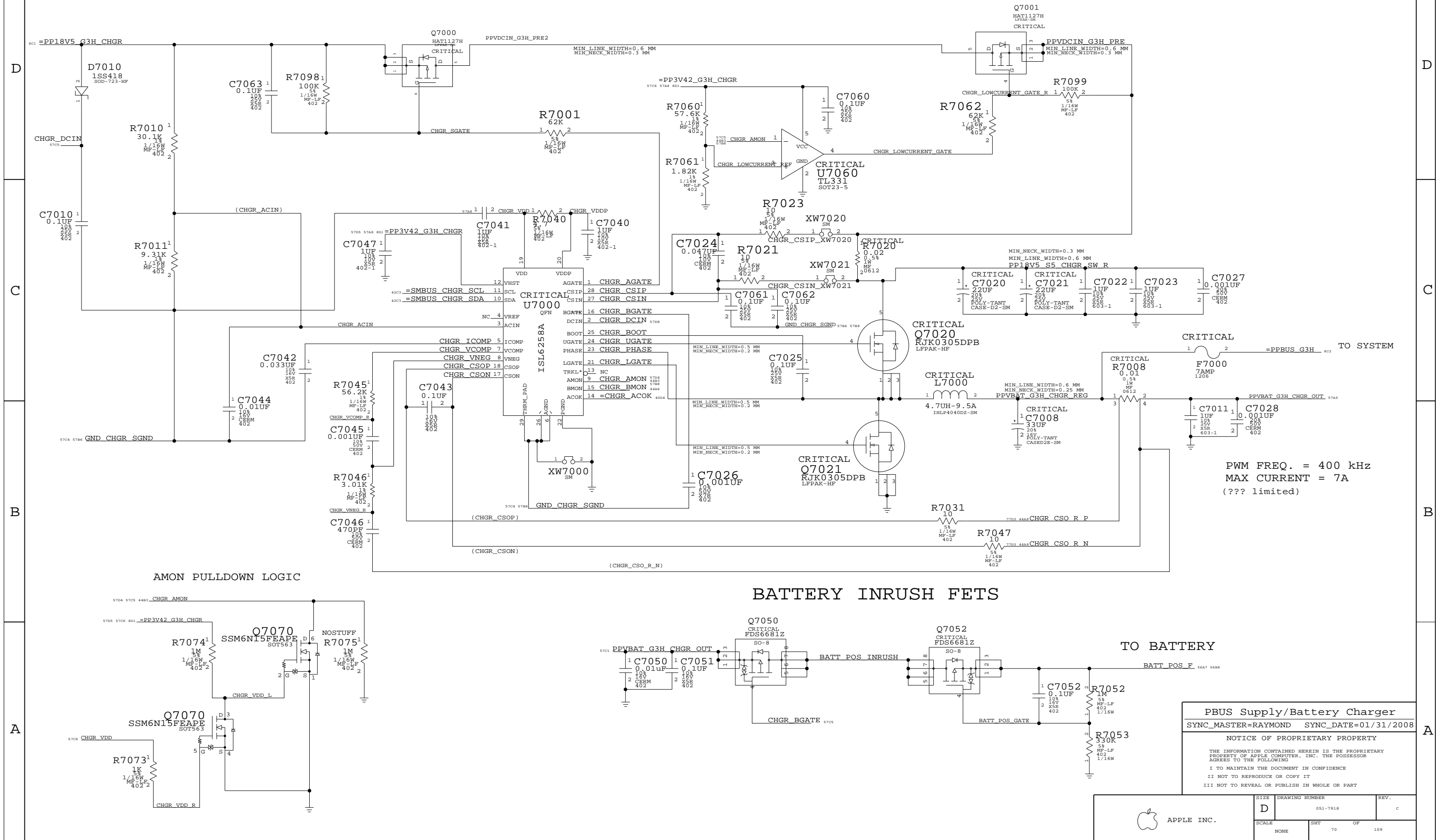








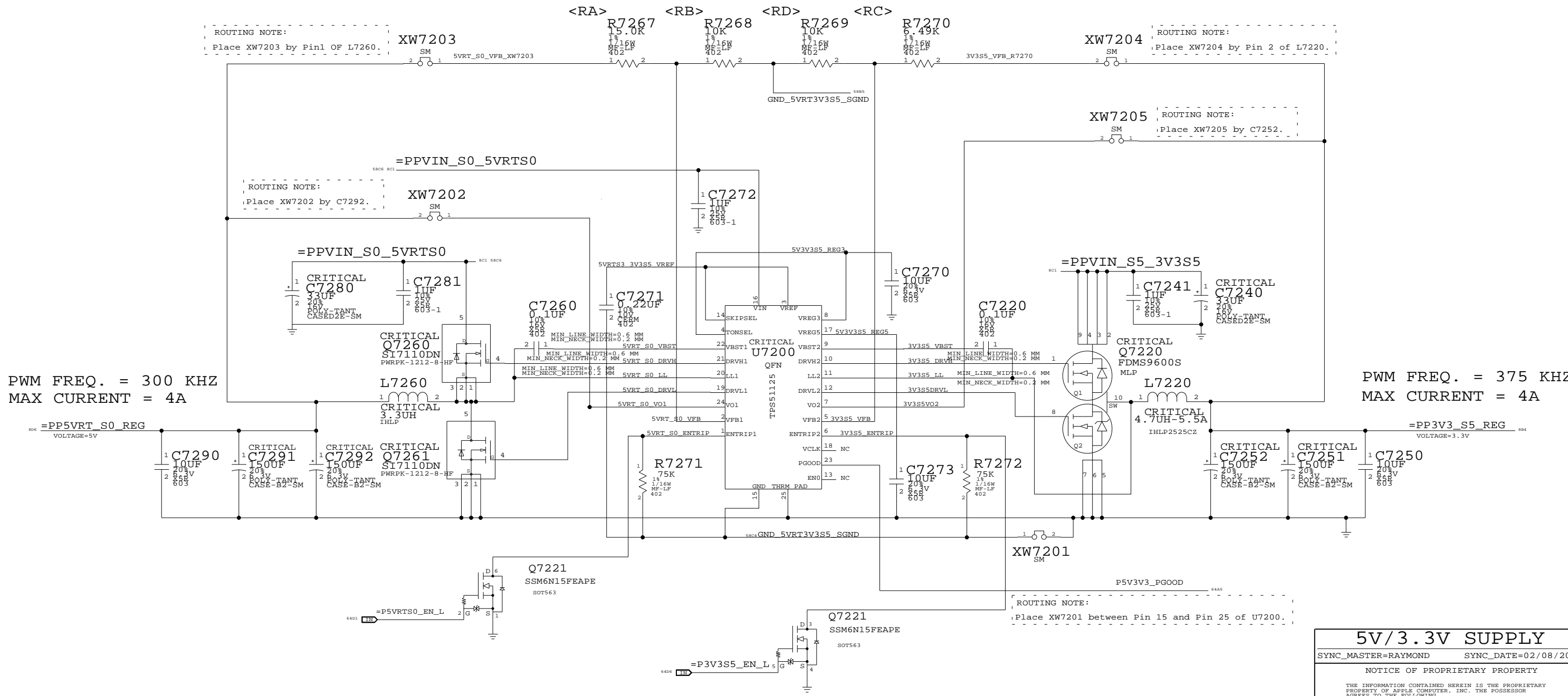
# PBUS SUPPLY / BATTERY CHARGER



# 5V\_RT/3.3V POWER SUPPLY

$V_{OUT} = (2 * R_A / R_B) + 2$

$V_{OUT} = (2 * R_C / R_D) + 2$



PWM FREQ. = 300 KHZ  
MAX CURRENT = 4A

PWM FREQ. = 375 KHZ  
MAX CURRENT = 4A

SEPERATED MASTER PG00D FOR BOTH 5V AND 3V3.

5V/3.3V SUPPLY

SYNC\_MASTER=RAYMOND

SYNC\_DATE=02/08/2008

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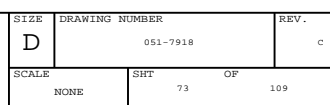
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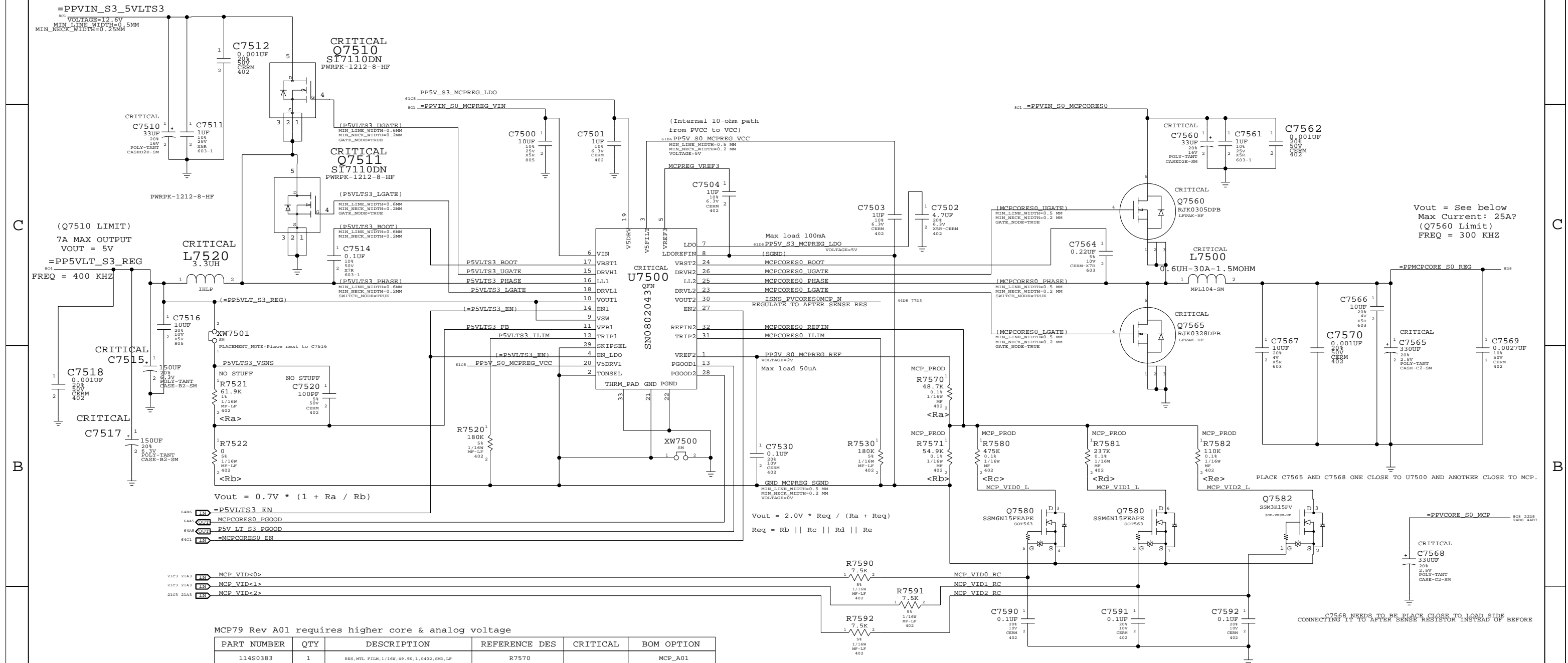
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	C
SCALE		SHT	OF
NONE		72	109

## D

BA



# MCP VCORE/5V\_S3 LEFT REGULATOR



MCP79 Rev A01 requires higher core & analog voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0383	1	RES,MTL FILM,1/16W,49.9K,1,0402,SMD,LF	R7570		MCP_A01
114S0401	1	RES,MTL FILM,1/16W,78.7K,1,0402,SMD,LF	R7571		MCP_A01
114S0484	1	RES,MTL FILM,1/16W,549K,1,0402,SMD,LF	R7580		MCP_A01
114S0454	1	RES,MTL FILM,1/16W,274K,1,0402,SMD,LF	R7581		MCP_A01
114S0423	1	RES,MTL FILM,1/16W,133K,1,0402,SMD,LF	R7582		MCP_A01
114S0373	1	RES,MTL FILM,1/16W,40.2K,1,0402,SMD,LF	R7570		MCP_A01P&MCP_A01Q
114S0404	1	RES,MTL FILM,1/16W,84.5K,1,0402,SMD,LF	R7571		MCP_A01P&MCP_A01Q
114S0458	1	RES,MTL FILM,1/16W,301K,1,0402,SMD,LF	R7580		MCP_A01P&MCP_A01Q
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R7581		MCP_A01P&MCP_A01Q
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7582		MCP_A01P&MCP_A01Q

VID<2:0>	Voltage	Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

MCP VCORE REGULATOR		
SYNC_MASTER=RAYMOND		SYNC_DATE=01/31/2008
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D	051-7918	C
SCALE	SHT	OF
NONE	75	109



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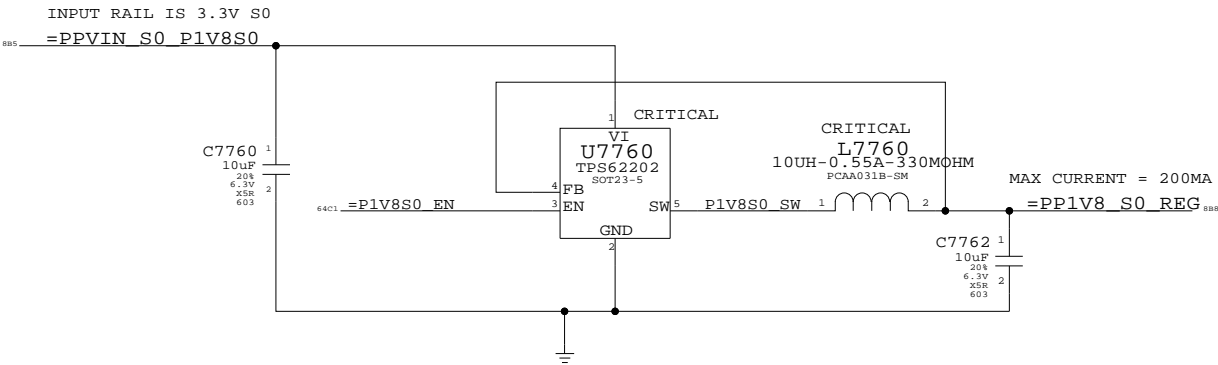
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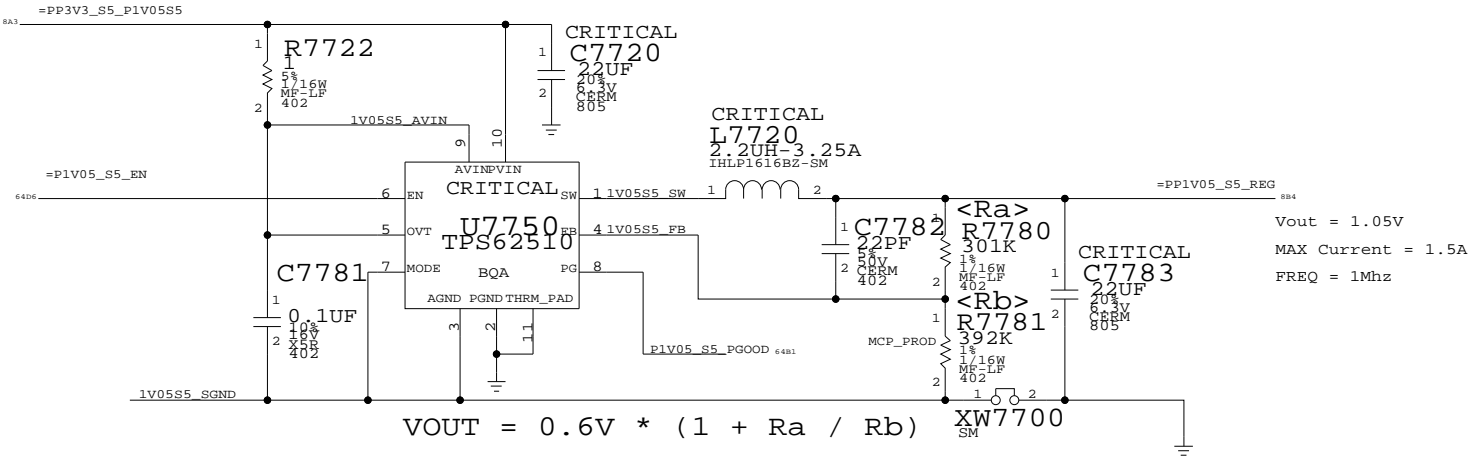
A

A APPLE INC.

1.8V S0 SWITCHER



MCP 1.05V\_S5 AUXC SUPPLY



MCP79 Rev A01 requires higher voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0464	1	RES,MTL FILM,1/16W,348K,1%,0402,SMD,LF	R7781	MCP_A01&MCP_A01P&MCP_A01Q	

MISC POWER SUPPLIES

SYNC\_MASTER=RAYMOND      SYNC\_DATE=01/23/2008

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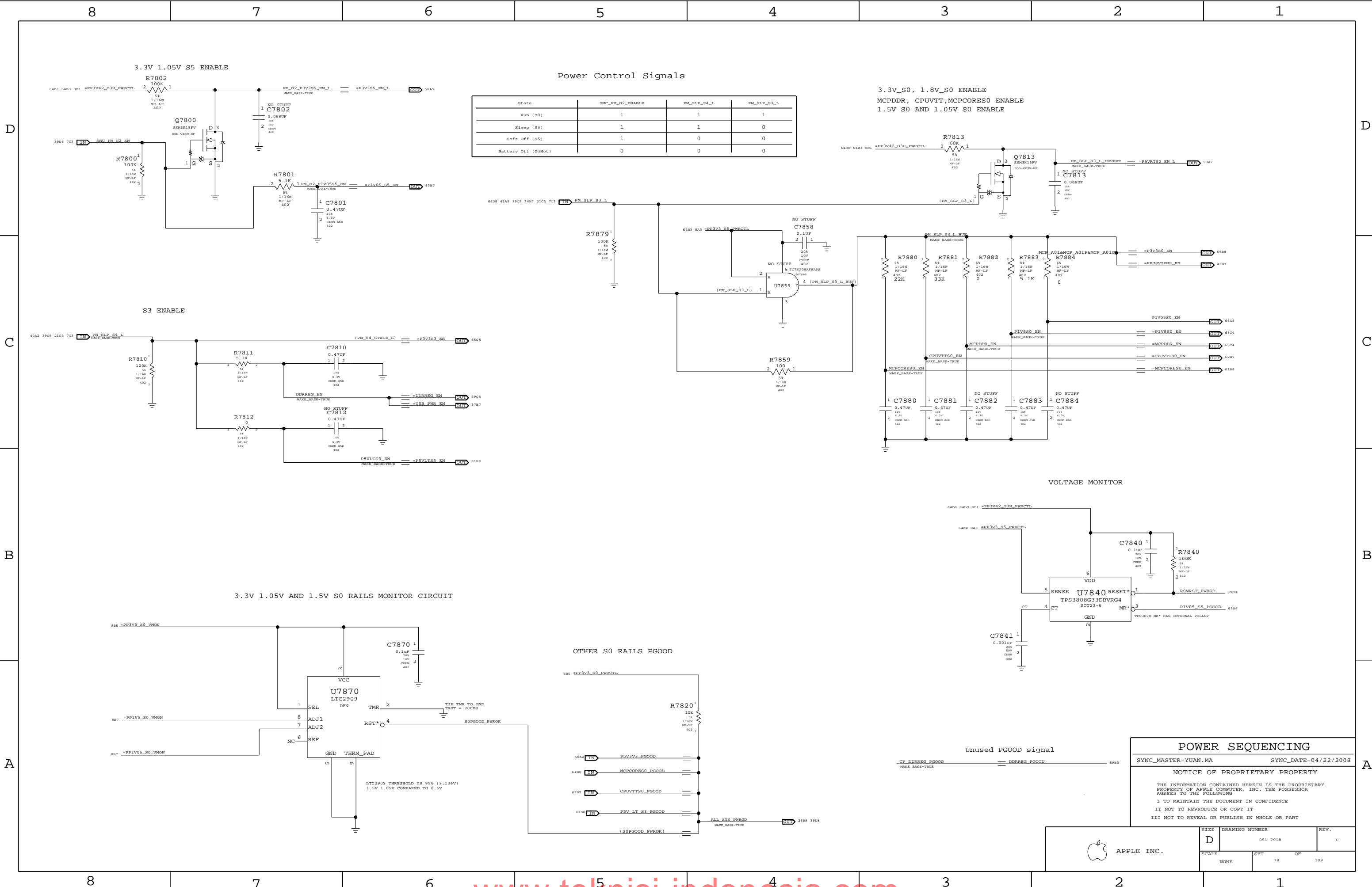
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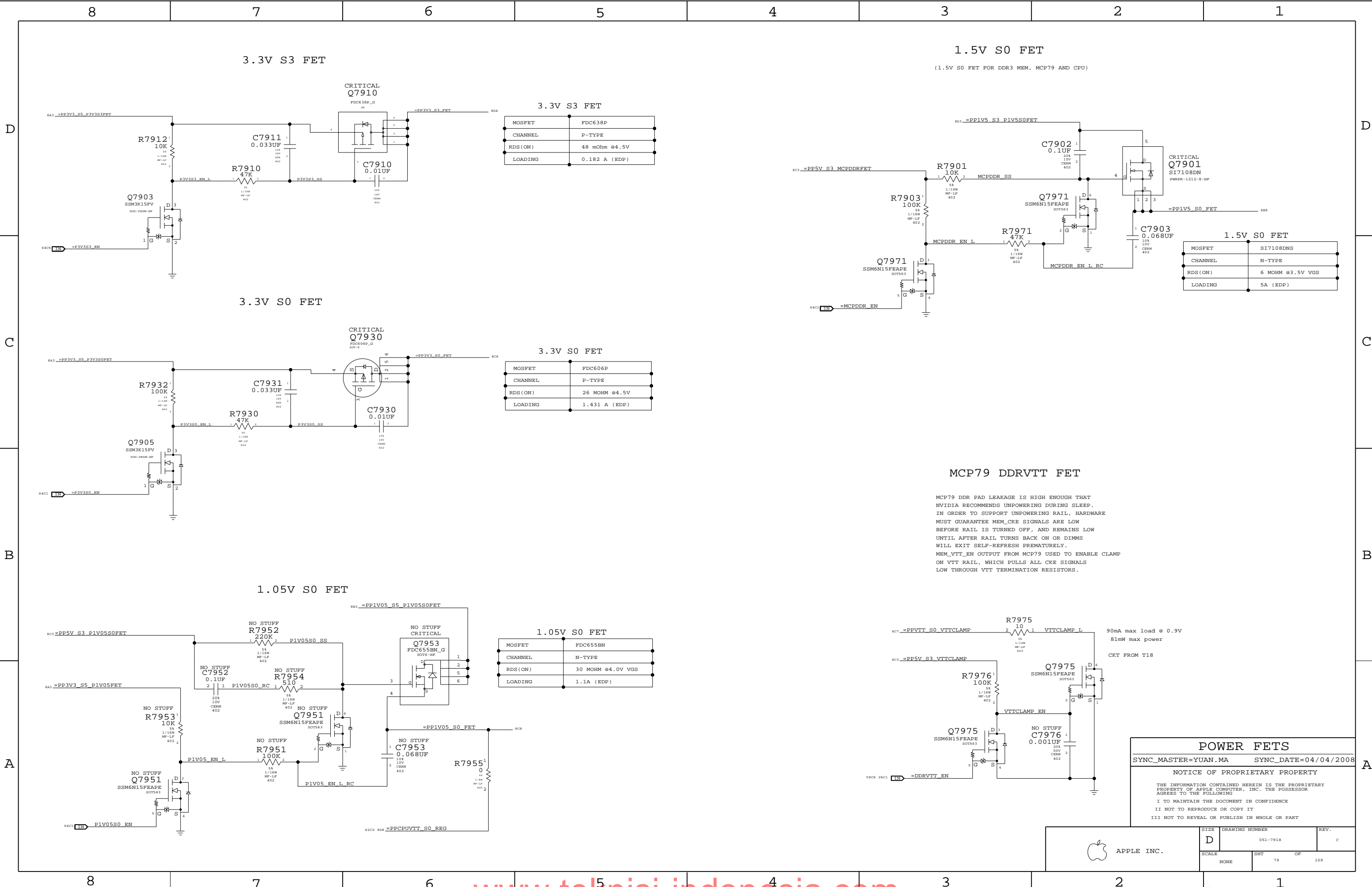
DRAWING NUMBER 051-7918

REV. c

SCALE NONE

SHT 77 OF 109





### 1.5V S0 FET

(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)

MOSFET	SI7108DNS
CHANNEL	N-TYPE
RDS(ON)	6 MOHM @3.5V VGS
LOADING	5A (EDP)

### MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM\_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM\_VTT\_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.

POWER FETS

SYNC\_MASTER=YUAN.MA    SYNC\_DATE=04/04/2008

NOTICE OF PROPRIETARY PROPERTY

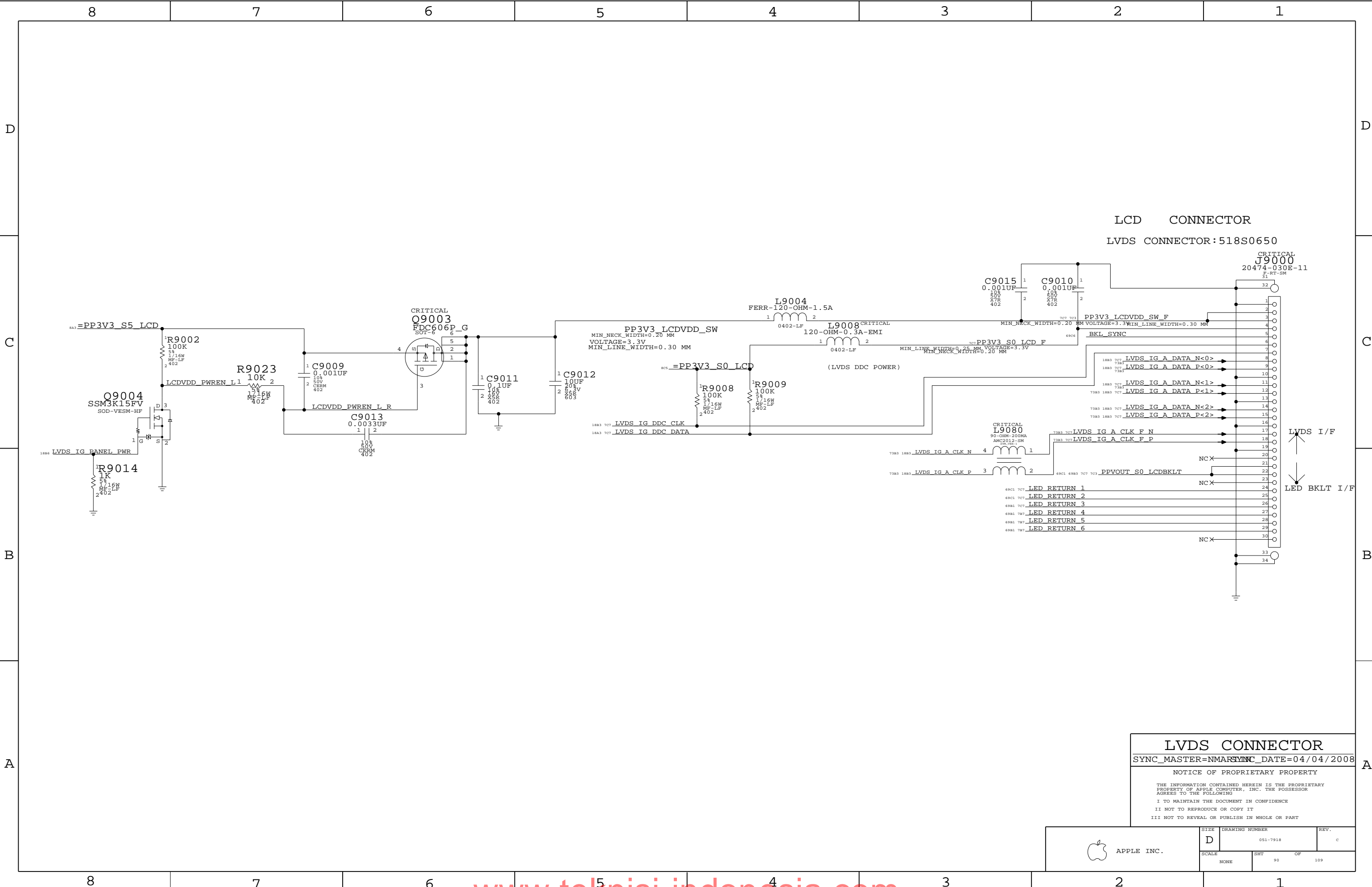
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	SCALE	SHT	OF
	NONE	79	109



LVDS CONNECTOR

SYNC\_MASTER=NMASSYNC\_DATE=04/04/2008


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	D	051-7918	c
SCALE	SHT OF 109		
NONE			

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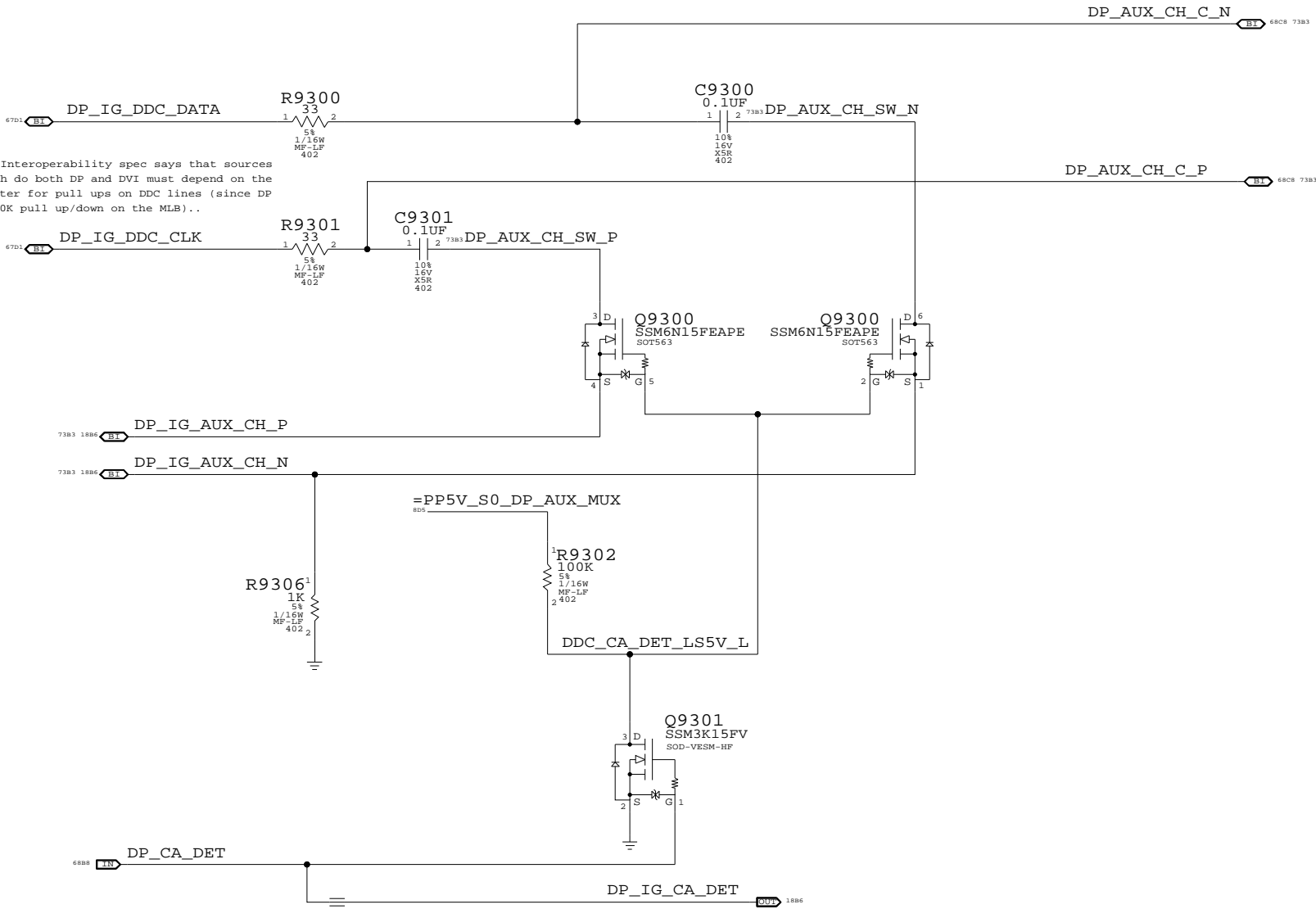
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Display Port Interoperability spec says that sources or sinks which do both DP and DVI must depend on the external adapter for pull ups on DDC lines (since DP AUX CH has 100K pull up/down on the MLB)..



1886	=MCP_HDMI_TXC_P	DP_ML_P<3>	68C8_73C3
1886	=MCP_HDMI_TXC_N	DP_ML_N<3>	MAKE_BASE=TRUE
1886	=MCP_HDMI_TXD_P<0>	DP_ML_P<2>	MAKE_BASE=TRUE
1886	=MCP_HDMI_TXD_N<0>	DP_ML_N<2>	MAKE_BASE=TRUE
1886	=MCP_HDMI_TXD_P<1>	DP_ML_P<1>	MAKE_BASE=TRUE
1886	=MCP_HDMI_TXD_N<1>	DP_ML_N<1>	MAKE_BASE=TRUE
1886	=MCP_HDMI_TXD_P<2>	DP_ML_P<0>	MAKE_BASE=TRUE
1886	=MCP_HDMI_TXD_N<2>	DP_ML_N<0>	MAKE_BASE=TRUE
1886	=MCP_HDMI_HPD	DP_HPD	MAKE_BASE=TRUE
18A3	=MCP_HDMI_DDC_CLK	DP_IG_DDC_CLK	MAKE_BASE=TRUE
18A3	=MCP_HDMI_DDC_DATA	DP_IG_DDC_DATA	MAKE_BASE=TRUE

## DISPLAYPORT SUPPORT

SYNC\_MASTER=AMASON SYNC\_DATE=04/18/2008

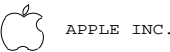
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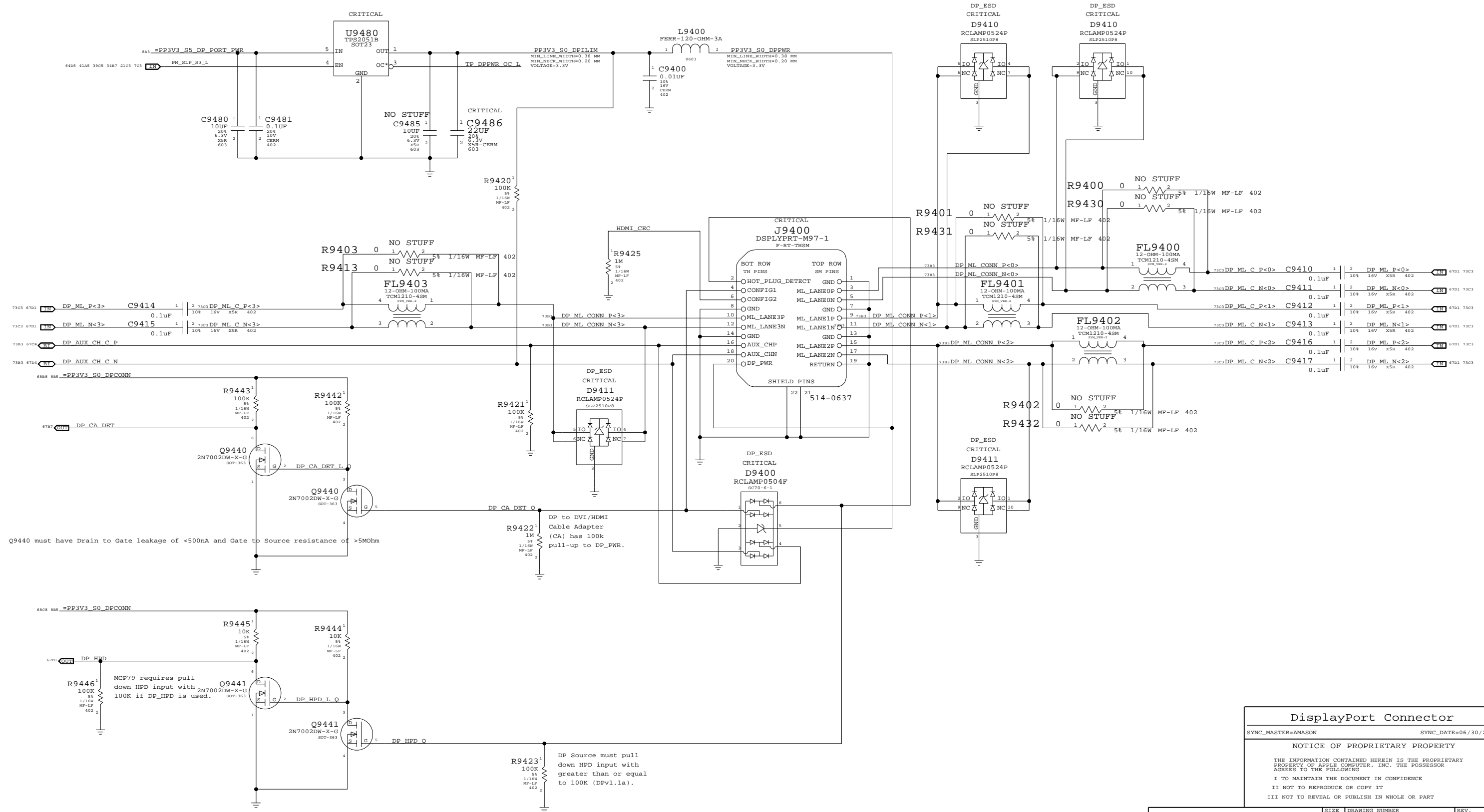
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	c
SCALE	SHT	OF
NONE	93	109

Port Power Switch



DisplayPort Connector

SYNC\_MASTER=AMASON SYNC\_DATE=06/30/2008

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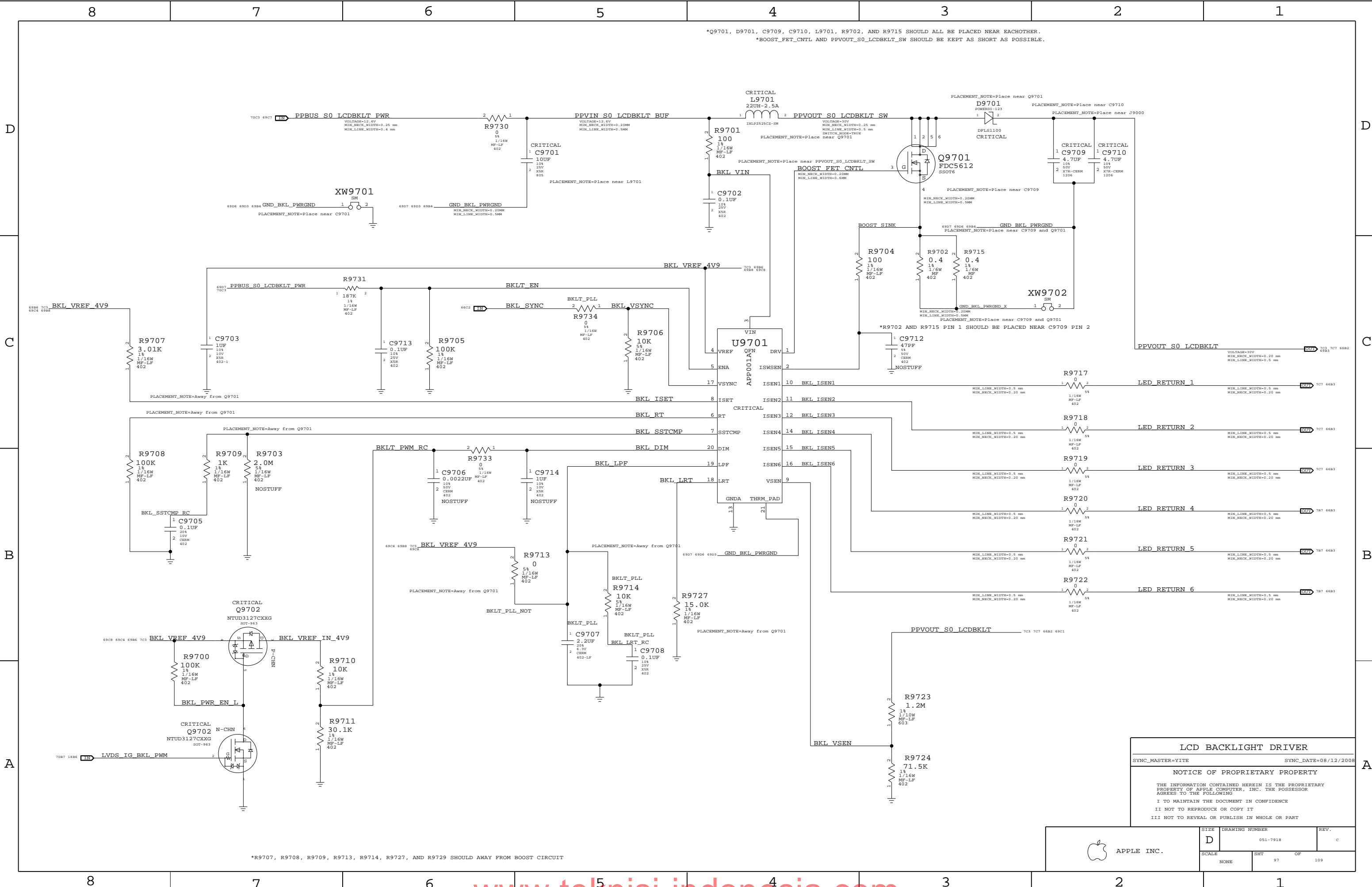
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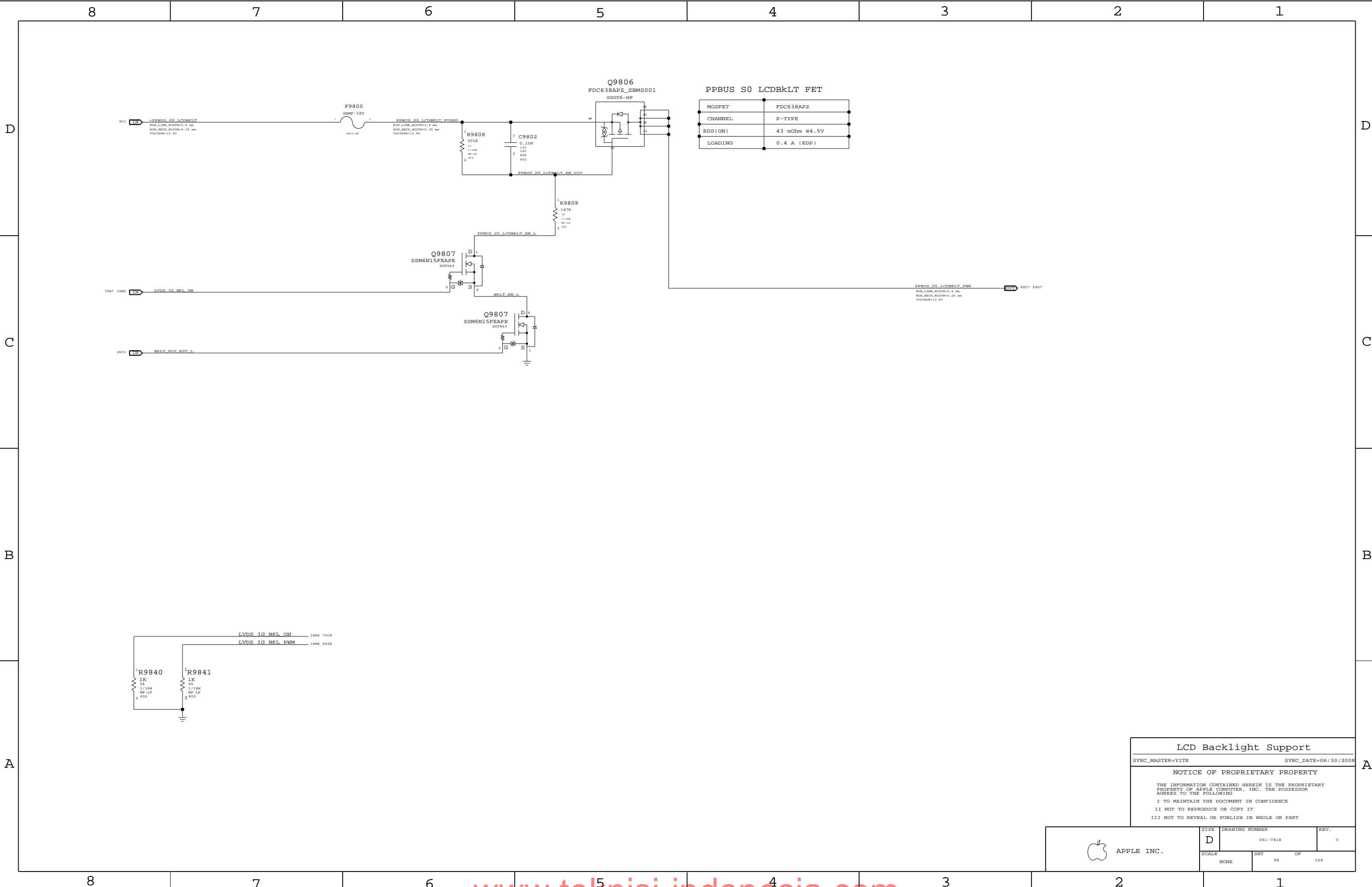
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	D	051-7918	C
SCALE	NONE	SHT	OF
		94	109





LCD Backlight Support

SYNC\_MASTER=YITESYNC\_DATE=06/30/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7918	c
SCALE		SHT	OF
NONE		98	109

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.  
Signals within each 4x group should be matched within 5 ps of strobe.  
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.  
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.  
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.  
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.  
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.  
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.  
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2  
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.  
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2  
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	10C4 14D3
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	10C4 14D6
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	10C4 14D6
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	10C4 14D6
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	1084 10C4 14C3 14D3
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	1084 14D6
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	1084 14D6
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	1084 14D6
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	10C2 1483 14C3
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	10C2 14D6
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	10C2 14D6
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	10C2 14D6
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	1082 10C2 1483
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	1082 14D6
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	1082 14D6
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	1082 14D6
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	10D8 14C6 14D6
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	10D8 1486
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	10D8 1486
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	10C8 10D8 14C6
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	10C8 1486
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	10D6 1486
FSB_BREQ0_1	FSB_50S	FSB_1X	FSB BREQ0 L	982 10D6 1486
FSB_BREQ1_1	FSB_50S	FSB_1X	FSB BREQ1 L	1486
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	10D6 1486
FSB_1X	FSB_50S	FSB_1X	FSB BPRI L	10D6 1483
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	10D6 1486
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	10D6 1483
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	10D6 1486
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	10D6 1486
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	10D6 1486
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	10D6 1486
FSB_CPURST_L	FSB_50S	FSB_1X	FSB CPURST L	982 10D6 13C2 14A3
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	10D6 14A6
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	10D6 1486
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L	10C8 14A3
CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>	9C2 1084
CPU_FERR_L	CPU_50S	CPU_SMIL	CPU FERR L	10C8 1487
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGNE L	10C8 14A3
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT L	10D6 14A3
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR	982 10C8 14A3
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI	982 1088 14A3
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L	10C5 1486 40D4 60C8
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD	1082 13C7 14A3
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L	1088 14A3
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L	10C8 14A3
PM_THRMTRIP_L	CPU_50S	CPU_SMIL	PM THRMTRIP L	10C6 1487 40C4
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB CPUSLP L	1082 14A3
CPU_FERR_SR	CPU_50S	CPU_AGTL	CPU DSLEP L	1082 14A3
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU DPRSTP L	9C2 1082 14A3 60C7
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L	1082 14A3
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14A6
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	1086 1483
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	1086 1483
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	13C3 1483
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	13C3 1483
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14A4
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14A4
CPU_FERR_L	CPU_50S		CPU IERR L	10D6
PM_DPRSLEPVR	CPU_50S	CPU_AGTL	PM DPRSLPVR	21C7 60D8
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLPVR	60C7
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	1084 2781
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	1083
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	1083
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	1083
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	1083
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI	6C6 1086 10C6 1383
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO	6C4 1086 10C6
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS	6C6 6C7 1086 10C6 1383
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK	6C6 6C7 10A6 10C6 1386
XDP_TRST_L	CPU_50S	CPU_ITP	XDP TRST L	6C6 6C7 10A6 10C6 1383
XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<4..0>	10C6 13C6
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP BPM L<5>	10C5 13C6
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST L	13C4
	CPU_50S	CPU_SMIL	CPU VID<6..0>	1186 60C7
	CPU_50S	CPU_SMIL	IMVP6 VID<6..0>	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	1185 60A5
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11A5 60A5
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	

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CPU/FSB Constraints

SYNC\_MASTER=T18\_MLB

SYNC\_DATE=01/04/2008

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051-7918

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SCALE

NONE

SHT

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OF

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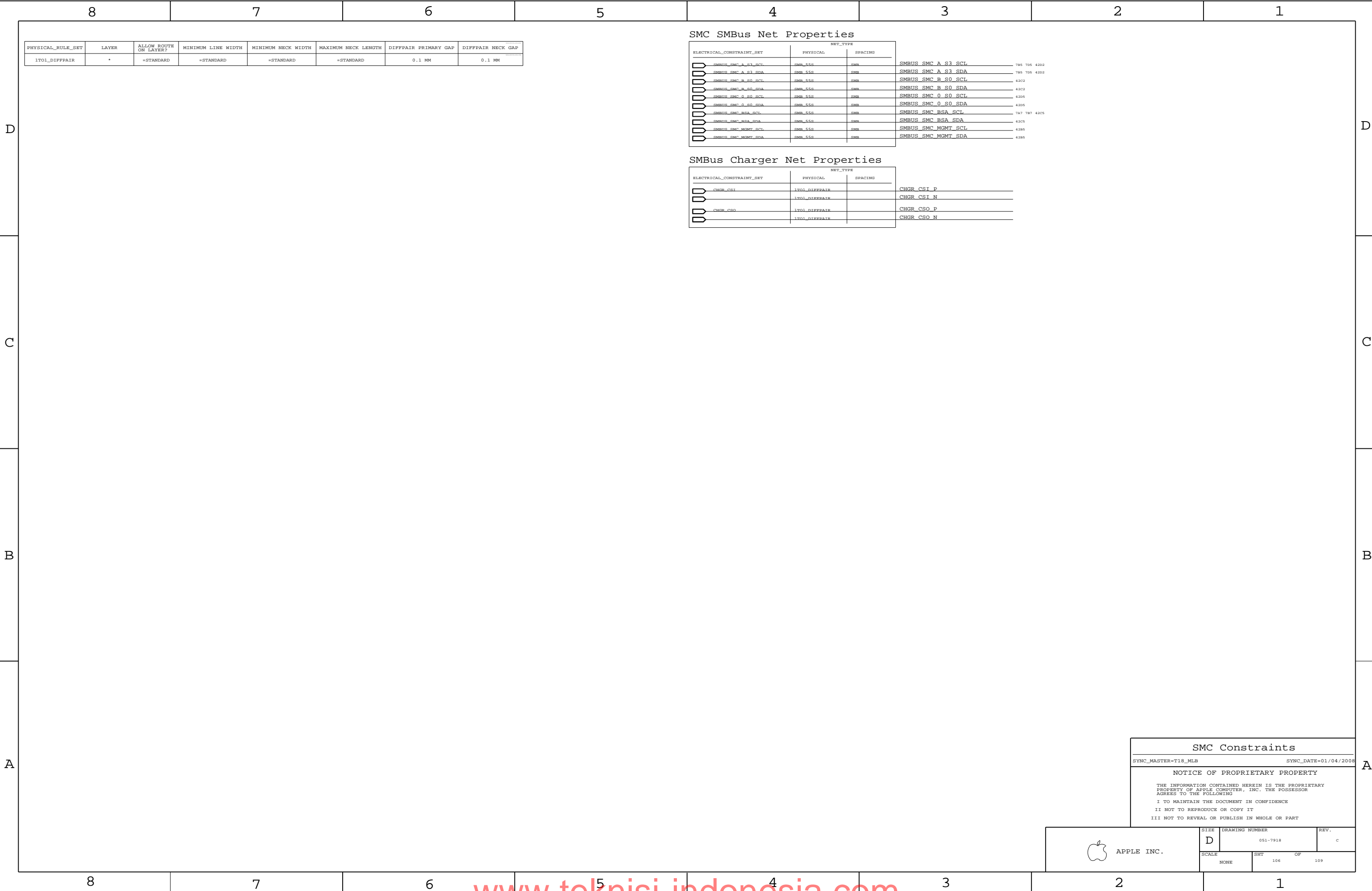
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8	7	6	5	4	3	2	1
M97 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA_P1MM		MM	15.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL3, ISL4, ISL9, ISL10	Y	0.083 MM	0.083 MM		0.400 MM	0.400 MM
100_OHM_DIFF_HDD	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
M97 RULE DEFINITIONS							
SYNC_MASTER=M97_MLB							
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